TNETV1056

Communications Processor for VoIP Phone Applications

Data Manual

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TEXAS INSTRUMENTS

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1 Features

- MIPS32™ 4KEc™ 32-Bit Reduced Instruction Set Computer (RISC) Processor
  - 125 MHz Providing up to 169 Dhrystone Million Instructions Per Second (MIPS)
  - 16K-Byte Four-Way Set Associative Instruction Cache
  - 16K-Byte Four-Way Set Associative Data Cache
  - Programmable Memory Management Unit (MMU)
  - 4K-Byte Random-Access Memory (RAM) On Chip
  - 4K-Byte Read-Only Memory (ROM) On Chip With Boot Code
  - Interrupt Handler
    - 40 Primary Interrupts With Programmable Priority
    - 5 Primary Interrupts May Be Sourced Externally
    - 32 Secondary Interrupts With Fixed Priority
  - Three 16-Bit Timers With Prescaled Clock
    - Two Universal Timers
    - One Dedicated Watchdog Timer
  - Enhanced JTAG IEEE Std 1149.1 Debug Interface
- Digital Signal Processor (DSP) C55x™
  - 100 MHz Providing up to 200 MIPS
  - 12K-Word Two-Way Set Associative Instruction Cache
  - 64K-Word RAM On Chip
    - 32K-Word Dual Access
    - 32K-Word Single Access
  - Interrupt Handler
  - Two 16-Bit Timers With Prescaled Clock
    - One Universal Timer
    - One Dedicated Watchdog Timer
  - Universal Four-Channel Direct Memory Access (DMA) Controller
  - Dedicated Peripheral DMA Controller
  - JTAG IEEE Std 1149.1 Debug Interface
- On-Chip Peripherals
  - External Memory Interface (EMIF) Supports:
    - Two SDRAM Chip Selects Providing 128M Byte
    - Three Chip Selects Providing 16M-Byte Each RAM or ROM
    - One Chip Select Providing 32M-Byte Flash
  - Universal Four-Channel DMA Controller
  - 52 General-Purpose Input/Output (GPIO) Signals
    - 8 GPIOs (Primary I/O Functions)
    - 44 GPIOs (Secondary I/O Functions)
  - Keypad Interface Featuring:
    - 8 × 8 Matrix Accommodating 64 Keys
    - Expanded Key Range With GPIO
    - Hardware Debounce Feature
  - Universal Asynchronous Receiver/Transmitter (UART) With Hardware Automatic Flow Control
  - Sequencer-Based Serial Port Providing Programmable Configuration for Standard Serial Interfaces
    - Serial Port Interface (SPI)
    - Inter-Integrated Circuit (I^2C™)
    - Microwire™
    - Numerous Standard and Nonstandard Variations
  - VLYNQ™ Serial Communications Port Featuring One 5-Terminal Port
  - Liquid Crystal Display (LCD) Controller Supports:
    - Alphanumeric Character Displays
    - Rasterized Graphic Displays up to 1024 × 1024 Pixels
    - Micro-Interface Graphic Displays
- Ethernet Subsystem
  - Ethernet Port Featuring:
    - Integrated IEEE Std 802.3/802.3u 10/100 Base-T PHY in Both Half and Full Duplex
      - Auto Negotiation
      - Parallel Detection
      - Support IEEE Std 802.3af Inline Power Through Glueless Connection to TI TPS2375
    - Integrated Ethernet Media Access Controller (MAC)
      - Full Duplex
      - Jumbo Packet
      - Copy Short/Error Frames
      - Hardware Flow Control
      - Address Filtering (Unicast, Multicast, Broadcast, or Promiscuous Mode)
    - External Media Independent Interface (MII) and LED Status Indicators Available
    - Remote Network Monitoring (RMO) Management Information Base (MIB) Statistics Gathering Registers

- **Integrated Voice Codec**
  - **Dual-Channel 16-Bit Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) units**
  - **Programmable Sampling Rate of 8 or 16 kHz**
  - **Selectable Finite Impulse Response/Infinite Impulse Response (FIR/IIR) Filter With Bypass Option**
  - **Five Inputs to the ADC**
  - **Four Outputs From the DAC**
  - **ADC Gain Programmable (0 to 54 dB)**
  - **DAC Gain Programmable (0 to –54 dB)**
  - **Analog and Digital Sidetone**
  - **81-dB Signal-to-Noise Ratio (SNR) for Each ADC**
  - **82-dB SNR for Each DAC**
  - **On-Chip Drivers for Handset, Headset, and Speakerphone**
- **Additional System Information**
  - **324-Terminal Plastic Ball Grid Array (PBGA) Package**
  - **3.3-V I/O Supply Input Voltage**
  - **Integrated Voltage Regulator for 1.5-V Core Supply**
  - **1.4-W Typical Power Consumption**

1.1 Description

The TNETV1056 is a communications processor consisting of a MIPS32™ reduced instruction set computer (RISC) processor and a C55x™ digital signal processor (DSP). This device has a rich peripheral set architected specifically for voice over internet protocol (VoIP) phone applications that results in a reduced bill of materials (BOM), reduced complexity, and reduced time to develop an internet protocol (IP) phone.

The TNETV1056 combines key processor, communication, and peripheral functions necessary to build a basic or advanced IP phone. The TNETV1056 architecture uses advanced design features to provide flexibility and performance throughput while reducing power consumption. Combined with Telogy Networks™ software for IP phone applications, the TNETV1056 provides a complete hardware/software solution capable of reducing system design cycle times.

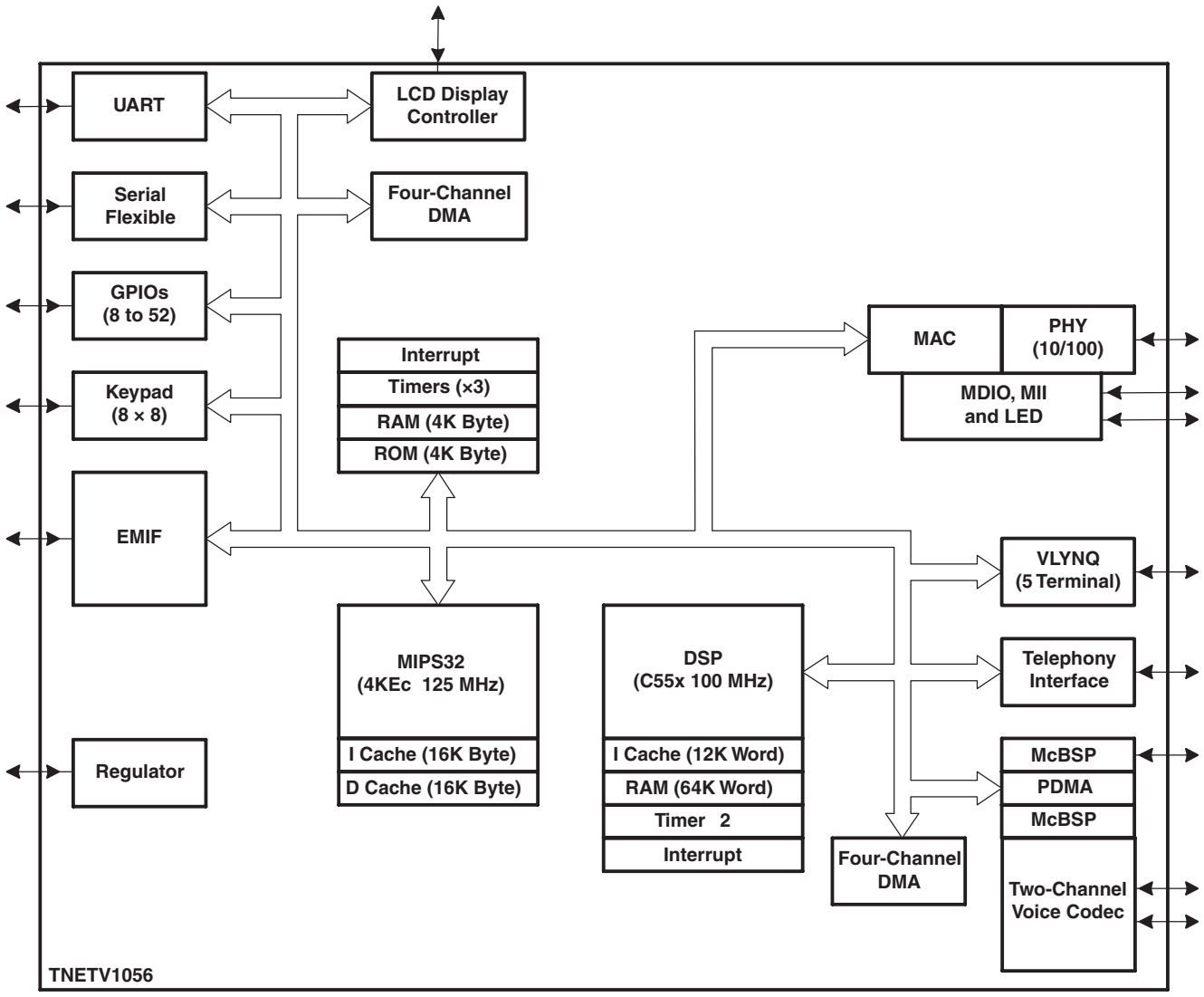
The RISC processor software supplies the overall system services and performs user interface, network management, protocol stack management, call processing, and task scheduling functions. The DSP software provides real-time voice processing functions such as echo cancellation, compression, pulse-code modulation (PCM) data processing, and tone generation and detection.

IP phone designs are simplified through the use of on-chip peripherals including a 16-bit color liquid crystal display (LCD) controller, 8 × 8 keypad interface, universal asynchronous receiver/transmitter (UART) serial interface, programmable serial port, VLYNQ interface, several GPIOs, a single 10/100 Base-T Ethernet media access controller (MAC) and physical interface (PHY), and integrated voltage regulator with advanced power management support.

The integrated dual-channel 16-bit voice coder/decoder (codec) integrates the critical functions needed for IP phone applications, including two analog-to-digital converters (ADCs) (with five programmable inputs) and two digital-to-analog converters (DACs) (with four programmable outputs). Other features include analog and digital sidetone control, an antialiasing filter, programmable gain options, a programmable sampling rate (8 kHz or 16 kHz), 8-Ω speaker driver, microphone, handset, and headset interfaces. In addition to the voice codec, an external multichannel buffered serial port (McBSP) serial interface and telephony interface provide glueless attachment to a wide variety of telephony peripherals.

1.2 TNETV1056 Functional Block Diagram

Figure 1-1 TNETV1056 Functional Block Diagram



2 Introduction

The TNETV1056 is a communications processor consisting of a MIPS32 RISC and a C55x DSP. Also included are integrated peripherals designed for VoIP phone applications.

The highly integrated features of the TNETV1056 support rapid implementation of VoIP phone solutions through software-differentiated control as described in the following items:

2.1 MIPS32 RISC processor

The MIPS32 processor functions as the master controller providing the overall system services, including the bootstrap loader and the real-time operating system (RTOS). This processor also performs network-manager, call-manager, and application-manager functions. The network manager handles standard network protocol stacks (H.323, SIP, and MGCP). The call manager handles telephony protocols including call setup and teardown. The application manager provides a control mechanism for interfaces and functions in the TNETV1056 that provide value beyond a basic telephony product (LCD, VLYNQ, UART, and serial port).

2.2 DSP

This DSP functions as the real-time voice controller. Activity for this processor includes PCM data reception, tone generation, acoustic echo cancellation/suppression, voice activity detection, voice playout, jitter buffer management, silence suppression, and a variety of voice-compression options. This processor has the capability to provide features for deluxe telephony products such as full-duplex speakerphones, three-way conferencing, wideband codec requirements, and fax requirements.

2.3 Ethernet subsystem

The integrated features of the Ethernet subsystem provide a complete Ethernet solution for telephony applications, including an IEEE Std 802.3 compliant MAC and an IEEE Std 802.3/802.3u compliant 10/100 Base-T physical layer device (PHY). Logical features supported by this Ethernet solution include IEEE Std 802.1p prioritization queues, IEEE Std 802.1D spanning tree protocol, IEEE Std 802.1Q virtual local area network (VLAN) support (both shared and independent), GARP multicast registration protocol (GMRP) support, and broadcast storm protection.

2.4 Integrated voice codec

The integrated features of this subsystem provide a complete telephony solution for voice and fax applications. Integrated into this subsystem is a complete two-channel voice codec capable of handling any deluxe three-way conferencing speakerphone application.

2.5 On-chip peripherals

The TNETV1056 includes a wide range of integrated peripherals that provide value beyond a basic processor. Included in this list of peripherals is an LCD controller capable of providing glueless attachment to a wide range of displays. The VLYNQ interface provides a standard high-speed serial interface to a variety of TI devices that can supplement the processing power or external connectivity of the TNETV1056. Additional serial port attachment is provided through the UART and sequencer serial port (SSP) interfaces. The SSP may be programmed to interface to a variety of standard (I^2C, SPI, or IDM-2) and nonstandard external serial devices.

3 Terminal Definitions

The TNETV1056 is packaged in a 324-terminal plastic ball grid array (PBGA). Package details are provided in section 6 "Mechanical Specification" on page 164. A top view of the 324-terminal PBGA package showing all of the primary TNETV1056 I/O primary function terminals is shown in Figure 3-1. In addition to the primary (1st) I/O functions shown in Figure 3-1, many TNETV1056 I/O terminals have secondary (2nd) functions (see Figure 3-2) or even tertiary (3rd) functions (see Figure 3-3). All of these multifunctional I/O terminals are listed by signal name in Table 3-2 and by terminal number in Table 3-3.

Figure 3-1 324-Terminal PBGA I/O Assignments, Primary Functions, Top View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	
22	VSS	VSS	EM_A19	EM_A16	EM_A12	EM_A08	EM_A05	EM_A02	TELE_CLK_O	TELE_RESET	TELE_RING_IN4	TELE_RING_IN2	REF_CLK_O	REF_CLK_I			VDDA_PHY1_1	P0_TX_M	P0_TX_P	VR_BASE3			22
21	VSS	VSS	EM_A20	EM_A17	EM_A13	EM_A09	EM_A06	EM_A03	EM_A00	TELE_INT	TELE_RING_IN3	TELE_RING_IN1	VSS_REF_CLK	ALT_CLK_I	VSS_PHY1_1	VSS_PHY1_1	VDDA_PHY0_1	VSS_PHY0_1	VSS_PHY0_1	PHY_TEST			21
20	EM_A23	EM_A22	VSS	EM_A18	EM_A14	EM_A10	EM_A07	EM_A04	EM_A01	TELE_CS	TELE_FS	TELE_DO	TELE_DI	VDDA_PHY1_34	VSS_PHY1_34	VSS_PHY1_2	VDDA_PHY0_2	VSS_PHY0_2	VSS_PHY0_34	VDDA_PHY0_34	P0_FDUP/LEX	P0_ACTI/VITY	20
19	EM_D01	EM_D00	EM_A21	VSS	EM_A15	EM_A11	VDDS	VDDS	VDDS	VDDS	TELE_CLK_I	TELE_DCLK	VDD_PLL			VSS_PHY1_ESD	VDDA_PHY1_2	VSS_PHY0_ESD	P0_RX_M	P0_RX_P	P0_LINK	P0_100MB	19
18	EM_D04	EM_D05	EM_D03	EM_D02															PHY_REF	PHY_REF_RTN	LCD_D15	LCD_D14	18
17	EM_D08	EM_D09	EM_D07	EM_D06															LCD_D13	LCD_D12	LCD_D11	LCD_D10	17
16	EM_D11	EM_D12	EM_D10	VDDS															VDDS	LCD_D09	LCD_D08	LCD_D07	16
15	EM_D14	EM_D15	EM_D13	VDDS															VDDS	LCD_D06	LCD_D05	LCD_D04	15
14	EM_D17	EM_D18	EM_D16	VDDS					VSS	VDD	VDD	VDD	VDD	VSS_PLL					VDDS	LCD_D03	LCD_D02	LCD_D01	14
13	EM_D20	EM_D21	EM_D19	VDDS					VDD	VSS	VSS	VSS	VSS	VDD					VDDS	LCD_D00	LCD_VSYNC_A	LCD_E1	13
12	EM_D24	EM_D25	EM_D23	EM_D22					VDD	VSS	VSS	VSS	VSS	VDD					LCD_HSYNC_W	LCD_PIXEL_STRB	LCD_BIAS_E0	KEYPAD15	12
11	EM_D28	EM_D29	EM_D27	EM_D26					VDD	VSS	VSS	VSS	VSS	VDD					KEYPAD13	KEYPAD14	KEYPAD12	KEYPAD11	11
10	EM_D30	EM_D31	EM_WE_DQM0	VDDS					VDD	VSS	VSS	VSS	VSS	VDD					VDDS	KEYPAD10	KEYPAD09	KEYPAD08	10
9	EM_WE_DQM3	EM_WE_DQM2	EM_WE_DQM1	VDDS					VSS	VDD	VDD	VDD	VDD	VSS_AIC_CLK					VDDS	KEYPAD07	KEYPAD06	KEYPAD05	9
8	EM_CS2	EM_CS1	EM_CS0	VDDS															VDDA_AIC	KEYPAD04	KEYPAD03	KEYPAD02	8
7	EM_CS5	EM_CS4	EM_CS3	VDDS															VDDA_AIC	AIC_DAC_6BIT	KEYPAD01	KEYPAD00	7
6	EM_RAS	EM_WAIT	EM_HIZ	EM_CLK															AIC_8_P	AIC_MIC_BIAS	VR_ENBL	VDD	6
5	EM_CAS	EM_OE	EM_RW	EM_CKE															AIC_8_M	AIC_HEAD_M	AIC_MIC_P	AIC_MIC_M	5
4	EM_WE	UART_RX	UART_TX	VSS	SSP3	TEST	VDDS	VDDS	VDDS	VDDS			VDDS	VDDS	VDDA_AIC	VDDA_AIC	AIC_150_M2	AIC_150_P2	VSS_AIC	AIC_HEAD_P	AIC_HAND_M	AIC_CALL_M	4
3	UART_RTS	UART_CTS	VSS	SSP0	EJTAG_DINT	EJTAG_TRST0	EJTAG_TDI	JTAG_EMU0	JTAG_TCK	VLYNQ5_CLK		McBSP_CLK_RX	McBSP_D_RX	McBSP_FS_TX	GPIO00	GPIO01	GPIO02	AIC_150_P1	AIC_150_M1	VSS_AIC	AIC_HAND_P	AIC_CALL_P	3
2	VSS	VSS	RE/SET_O	SSP2	EJTAG_SYSRST	EJTAG_TCK	EJTAG_TMS	JTAG_TRST	JTAG_TDO	VLYNQ5_RX_D0	VLYNQ5_TX_D0		McBSP_CLK_TX	McBSP_FS_RX	VR_BASE2	GPIO03	GPIO04	GPIO05	AIC_LINE_P	AIC_LINE_M	VSS_AIC	VSS_AIC	2
1	VSS	VSS	RE/SET_I	SSP1	EJTAG_TRST1	EJTAG_TDO	JTAG_EMU1	JTAG_TDI	JTAG_TMS	VLYNQ5_RX_D1	VLYNQ5_TX_D1			McBSP_D_TX	AIC_CLK_I	AIC_CLK_O	GPIO06	GPIO07	AIC_600_P	AIC_600_M	VSS_AIC	VSS_AIC	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	

Figure 3-2 324-Terminal PBGA I/O Assignments, Secondary Functions, Top View

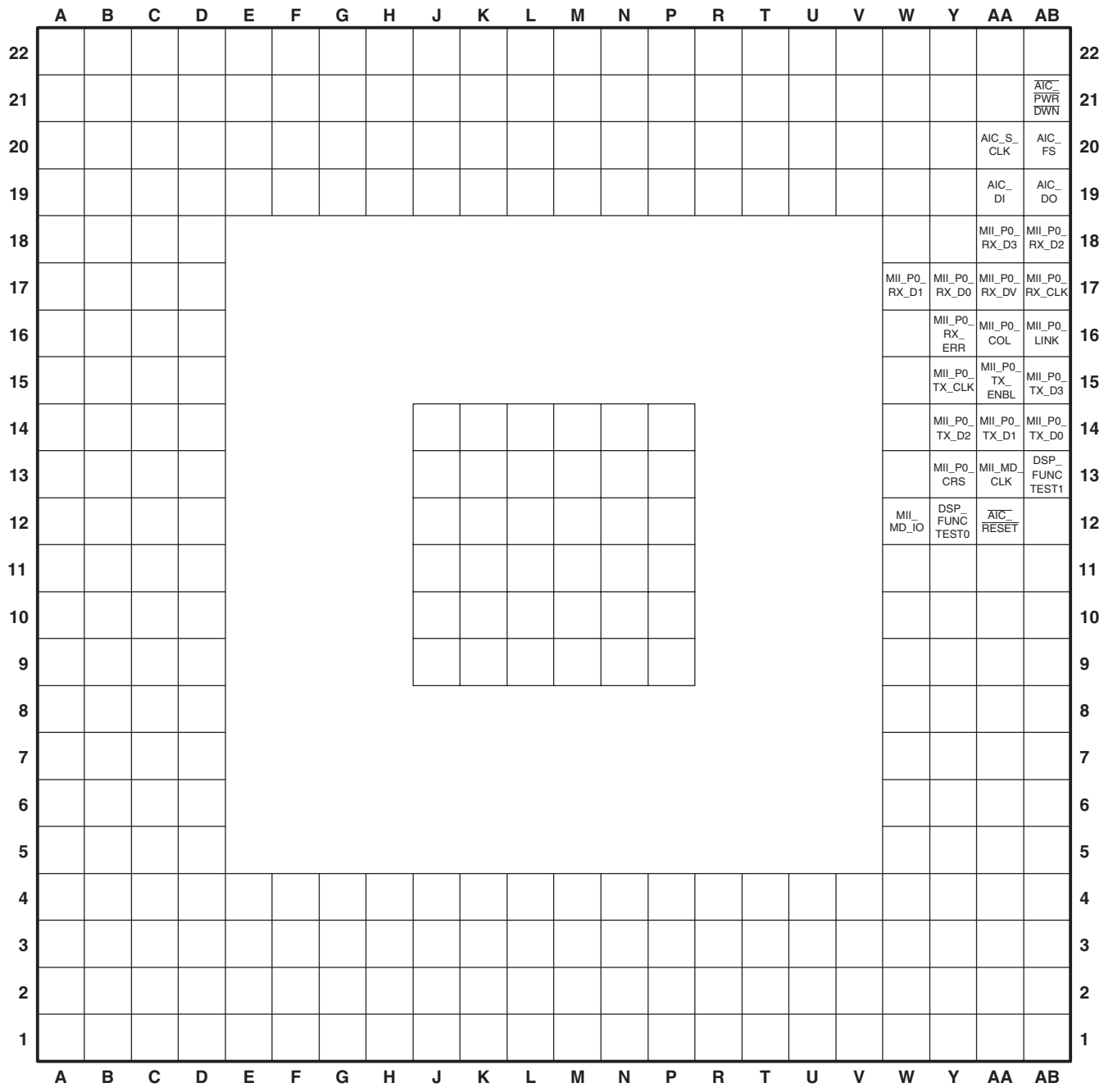
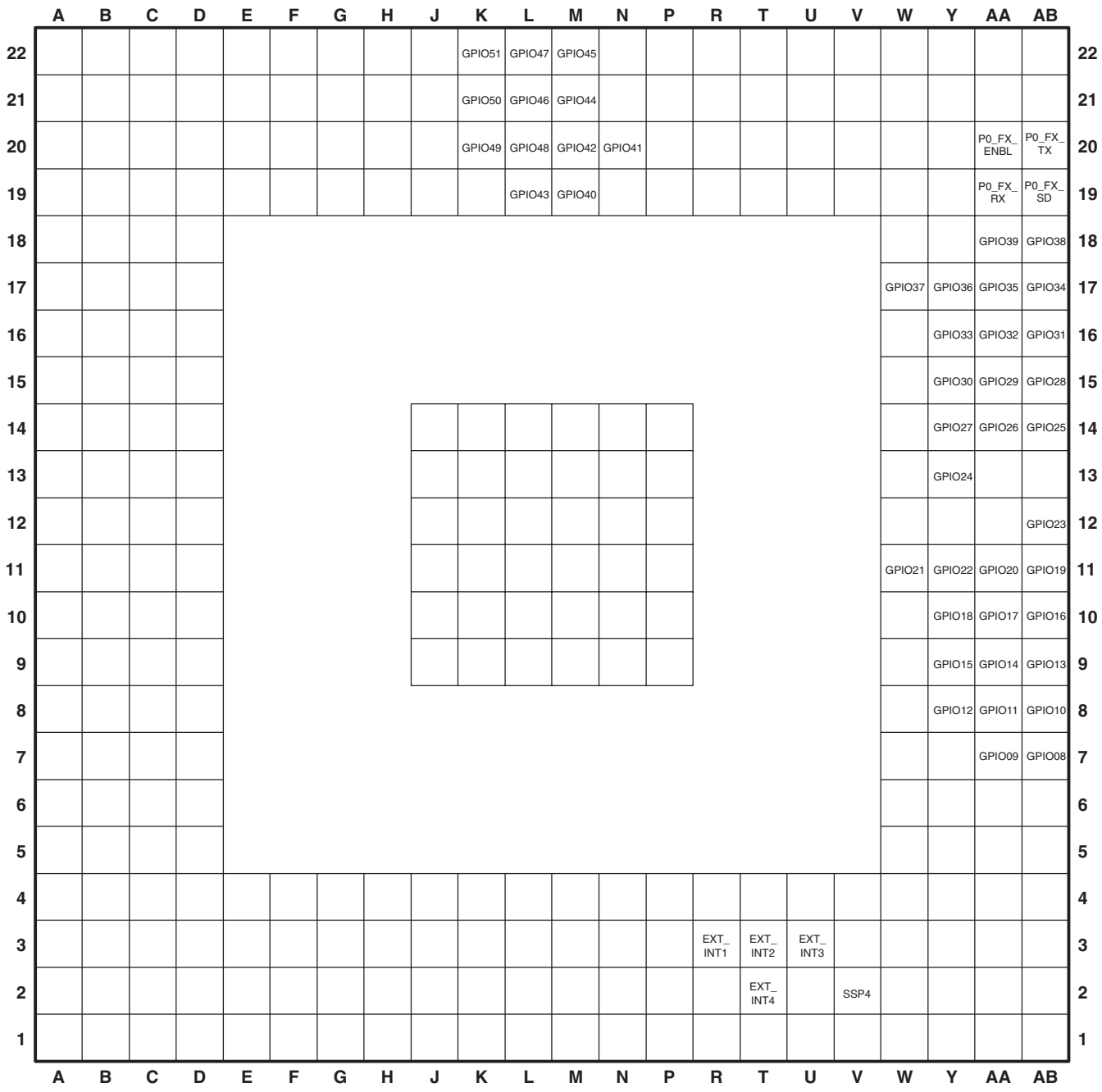


Figure 3-3 324-Terminal PBGA I/O Assignments, Tertiary Functions, Top View



3.1 Functional Symbol Definitions

Use the following functional symbol definitions when reading section 3.2 "Terminal Assignments" on page 20 and section 3.3 "Signal Descriptions" on page 33.

Table 3-1 I/O Functional Symbol Definitions

Functional Symbol	Definition	Table 3-3 Column Headings
4	4-mA source and 4-mA sink for the defined output driver	Drive Current
8	8-mA source and 8-mA sink for the defined output driver	Drive Current
_DI	Indicates an input terminal	Signal Name
_DO	Indicates an output terminal	Signal Name
_I	Indicates an input terminal	Signal Name
_M	Indicates the minus input or output terminal for a differential pair	Signal Name
_O	Indicates an output terminal	Signal Name
_P	Indicates the plus input or output terminal for a differential pair	Signal Name
1.5-V core	Core input power, typically supplied at 1.5 V by the internal voltage regulator	Other
3.3-V I/O	I/O input power, typically 3.3 V	Other
analog	Analog input terminal that may have special needs	Other
D	Internal 100-µA pulldown provided for this terminal	Pull Up/Down
FS	Provides a fail-safe feature to the input receiver or output driver. The fail-safe feature provides power-down protection for TNETV1056 I/Os connected to an actively powered-up external device. This allows the fail-safe terminal to be driven above its own supply-voltage level. A fail-safe terminal has no diodes to the power-supply rail, which ensures that no current flows into the terminal if a signal is applied when VDD or VDDS are 0 V (powered down).	Fail Safe
G	Ground input voltage terminal highlighting both digital and analog grounds	Type
GND	Ground input voltage, typically 0 V	Other
GND analog	Analog ground input voltage, typically 0 V, that may have special needs	Other
I	Input	Type
LN	Provides a low-noise feature to the defined output driver	Low Noise
N/C	No connection. Do not bias or use as a routing point. These terminals may be connected internally.	Signal Name
O	Output	Type
oscillator	Special oscillator I/O terminals	Other
P	Power input voltage terminal highlighting I/O (3.3 V), core (1.5 V), and analog voltages	Type
u	Internal 20-µA pullup provided for this terminal, with power supplied from VDDS (3.3-V I/O power)	Pull Up/Down
U	Internal 100-µA pullup provided for this terminal, with power supplied from VDDS (3.3-V I/O power)	Pull Up/Down
V analog	Analog input power that may have special needs	Other
V regulator	Special voltage regulator I/O terminals	Other
End of Table 3-1		

3.2 Terminal Assignments

Table 3-2 Terminal Assignments by Signal Name

Terminal (Part 1 of 10)		
Name	**Fn[1]**	**No.**
AIC_150_M1	1st	W3
AIC_150_M2	1st	U4
AIC_150_P1	1st	V3
AIC_150_P2	1st	V4
AIC_600_M	1st	Y1
AIC_600_P	1st	W1
AIC_8_M	1st	W5
AIC_8_P	1st	W6
AIC_CALL_M	1st	AB4
AIC_CALL_P	1st	AB3
AIC_CLK_I	1st	R1
AIC_CLK_O	1st	T1
AIC_DAC_6BIT	1st	Y7
AIC_DI	2nd	AA19
AIC_DO	2nd	AB19
AIC_FS	2nd	AB20
AIC_HAND_M	1st	AA4
AIC_HAND_P	1st	AA3
AIC_HEAD_M	1st	Y5
AIC_HEAD_P	1st	Y4
AIC_LINE_M	1st	Y2
AIC_LINE_P	1st	W2
AIC_MIC_BIAS	1st	Y6
AIC_MIC_M	1st	AB5
AIC_MIC_P	1st	AA5
$\overline{\text{AIC\_PWRDWN}}$	2nd	AB21
$\overline{\text{AIC\_RESET}}$	2nd	AA12
AIC_S_CLK	2nd	AA20
ALT_CLK_I	1st	P21
DSP_FUNCTEST0	2nd	Y12
DSP_FUNCTEST1	2nd	AB13
EJTAG_DINT	1st	E3
$\overline{\text{EJTAG\_SYSRST}}$	1st	E2
EJTAG_TCK	1st	F2
EJTAG_TDI	1st	G3
EJTAG_TDO	1st	F1
EJTAG_TMS	1st	G2
$\overline{\text{EJTAG\_TRST0}}$	1st	F3

Terminal (Part 2 of 10)		
Name	**Fn[1]**	**No.**
$\overline{\text{EJTAG\_TRST1}}$	1st	E1
EM_A00	1st	J21
EM_A01	1st	J20
EM_A02	1st	H22
EM_A03	1st	H21
EM_A04	1st	H20
EM_A05	1st	G22
EM_A06	1st	G21
EM_A07	1st	G20
EM_A08	1st	F22
EM_A09	1st	F21
EM_A10	1st	F20
EM_A11	1st	F19
EM_A12	1st	E22
EM_A13	1st	E21
EM_A14	1st	E20
EM_A15	1st	E19
EM_A16	1st	D22
EM_A17	1st	D21
EM_A18	1st	D20
EM_A19	1st	C22
EM_A20	1st	C21
EM_A21	1st	C19
EM_A22	1st	B20
EM_A23	1st	A20
$\overline{\text{EM\_CAS}}$	1st	A5
EM_CKE	1st	D5
EM_CLK	1st	D6
$\overline{\text{EM\_CS0}}$	1st	C8
$\overline{\text{EM\_CS1}}$	1st	B8
$\overline{\text{EM\_CS2}}$	1st	A8
$\overline{\text{EM\_CS3}}$	1st	C7
$\overline{\text{EM\_CS4}}$	1st	B7
$\overline{\text{EM\_CS5}}$	1st	A7
EM_D00	1st	B19
EM_D01	1st	A19
EM_D02	1st	D18
EM_D03	1st	C18
EM_D04	1st	A18

Terminal (Part 3 of 10)		
Name	**Fn[1]**	**No.**
EM_D05	1st	B18
EM_D06	1st	D17
EM_D07	1st	C17
EM_D08	1st	A17
EM_D09	1st	B17
EM_D10	1st	C16
EM_D11	1st	A16
EM_D12	1st	B16
EM_D13	1st	C15
EM_D14	1st	A15
EM_D15	1st	B15
EM_D16	1st	C14
EM_D17	1st	A14
EM_D18	1st	B14
EM_D19	1st	C13
EM_D20	1st	A13
EM_D21	1st	B13
EM_D22	1st	D12
EM_D23	1st	C12
EM_D24	1st	A12
EM_D25	1st	B12
EM_D26	1st	D11
EM_D27	1st	C11
EM_D28	1st	A11
EM_D29	1st	B11
EM_D30	1st	A10
EM_D31	1st	B10
EM_HIZ	1st	C6
$\overline{\text{EM\_OE}}$	1st	B5
EM_R/$\overline{\text{W}}$	1st	C5
$\overline{\text{EM\_RAS}}$	1st	A6
EM_WAIT	1st	B6
$\overline{\text{EM\_WE}}$	1st	A4
$\overline{\text{EM\_WE\_DQM0}}$	1st	C10
$\overline{\text{EM\_WE\_DQM1}}$	1st	C9
$\overline{\text{EM\_WE\_DQM2}}$	1st	B9
$\overline{\text{EM\_WE\_DQM3}}$	1st	A9
EXT_INT1	3rd	R3
EXT_INT2	3rd	T3

Terminal (Part 4 of 10)		
Name	**Fn[1]**	**No.**
EXT_INT3	3rd	U3
EXT_INT4	3rd	T2
GPIO00	1st	R3
GPIO01	1st	T3
GPIO02	1st	U3
GPIO03	1st	T2
GPIO04	1st	U2
GPIO05	1st	V2
GPIO06	1st	U1
GPIO07	1st	V1
GPIO08	3rd	AB7
GPIO09	3rd	AA7
GPIO10	3rd	AB8
GPIO11	3rd	AA8
GPIO12	3rd	Y8
GPIO13	3rd	AB9
GPIO14	3rd	AA9
GPIO15	3rd	Y9
GPIO16	3rd	AB10
GPIO17	3rd	AA10
GPIO18	3rd	Y10
GPIO19	3rd	AB11
GPIO20	3rd	AA11
GPIO21	3rd	W11
GPIO22	3rd	Y11
GPIO23	3rd	AB12
GPIO24	3rd	Y13
GPIO25	3rd	AB14
GPIO26	3rd	AA14
GPIO27	3rd	Y14
GPIO28	3rd	AB15
GPIO29	3rd	AA15
GPIO30	3rd	Y15
GPIO31	3rd	AB16
GPIO32	3rd	AA16
GPIO33	3rd	Y16
GPIO34	3rd	AB17
GPIO35	3rd	AA17
GPIO36	3rd	Y17
GPIO37	3rd	W17
GPIO38	3rd	AB18

Terminal (Part 5 of 10)		
Name	**Fn[1]**	**No.**
GPIO39	3rd	AA18
GPIO40	3rd	M19
GPIO41	3rd	N20
GPIO42	3rd	M20
GPIO43	3rd	L19
GPIO44	3rd	M21
GPIO45	3rd	M22
GPIO46	3rd	L21
GPIO47	3rd	L22
GPIO48	3rd	L20
GPIO49	3rd	K20
GPIO50	3rd	K21
GPIO51	3rd	K22
JTAG_EMU0	1st	H3
JTAG_EMU1	1st	G1
JTAG_TCK	1st	J3
JTAG_TDI	1st	H1
JTAG_TDO	1st	J2
JTAG_TMS	1st	J1
$\overline{\text{JTAG\_TRST}}$	1st	H2
KEYPAD00	1st	AB7
KEYPAD01	1st	AA7
KEYPAD02	1st	AB8
KEYPAD03	1st	AA8
KEYPAD04	1st	Y8
KEYPAD05	1st	AB9
KEYPAD06	1st	AA9
KEYPAD07	1st	Y9
KEYPAD08	1st	AB10
KEYPAD09	1st	AA10
KEYPAD10	1st	Y10
KEYPAD11	1st	AB11
KEYPAD12	1st	AA11
KEYPAD13	1st	W11
KEYPAD14	1st	Y11
KEYPAD15	1st	AB12
LCD_BIAS_E0	1st	AA12
LCD_D00	1st	Y13
LCD_D01	1st	AB14
LCD_D02	1st	AA14
LCD_D03	1st	Y14

Terminal (Part 6 of 10)		
Name	**Fn[1]**	**No.**
LCD_D04	1st	AB15
LCD_D05	1st	AA15
LCD_D06	1st	Y15
LCD_D07	1st	AB16
LCD_D08	1st	AA16
LCD_D09	1st	Y16
LCD_D10	1st	AB17
LCD_D11	1st	AA17
LCD_D12	1st	Y17
LCD_D13	1st	W17
LCD_D14	1st	AB18
LCD_D15	1st	AA18
LCD_E1	1st	AB13
$\overline{\text{LCD\_HSYNC\_W}}$	1st	W12
LCD_PIXEL_STRB	1st	Y12
LCD_VSYNC_A	1st	AA13
McBSP_CLK_RX	1st	M3
McBSP_CLK_TX	1st	N2
McBSP_D_RX	1st	N3
McBSP_D_TX	1st	P1
McBSP_FS_RX	1st	P2
McBSP_FS_TX	1st	P3
MII_MD_CLK	2nd	AA13
MII_MD_IO	2nd	W12
MII_P0_COL	2nd	AA16
MII_P0_CRS	2nd	Y13
MII_P0_LINK	2nd	AB16
MII_P0_RX_CLK	2nd	AB17
MII_P0_RX_D0	2nd	Y17
MII_P0_RX_D1	2nd	W17
MII_P0_RX_D2	2nd	AB18
MII_P0_RX_D3	2nd	AA18
MII_P0_RX_DV	2nd	AA17
MII_P0_RX_ERR	2nd	Y16
MII_P0_TX_CLK	2nd	Y15
MII_P0_TX_D0	2nd	AB14
MII_P0_TX_D1	2nd	AA14
MII_P0_TX_D2	2nd	Y14
MII_P0_TX_D3	2nd	AB15
MII_P0_TX_ENBL	2nd	AA15
$\overline{\text{P0\_100MB}}$	1st	AB19

Terminal (Part 7 of 10)		
Name	**Fn[1]**	**No.**
P0_ACTIVITY	1st	AB20
P0_FDUPLEX	1st	AA20
P0_FX_ENBL	3rd	AA20
P0_FX_RX	3rd	AA19
P0_FX_SD	3rd	AB19
P0_FX_TX	3rd	AB20
P0_LINK	1st	AA19
P0_RX_M	1st	W19
P0_RX_P	1st	Y19
P0_TX_M	1st	V22
P0_TX_P	1st	W22
PHY_REF	1st	W18
PHY_REF_RTN	1st	Y18
PHY_TEST	1st	Y21
REF_CLK_I	1st	P22
REF_CLK_O	1st	N22
RESET_I	1st	C1
RESET_O	1st	C2
SSP0	1st	D3
SSP1	1st	D1
SSP2	1st	D2
SSP3	1st	E4
SSP4	3rd	V2
TELE_CLK_I	1st	L19
TELE_CLK_O	1st	J22
TELE_CS	1st	K20
TELE_DCLK	1st	M19
TELE_DI	1st	N20
TELE_DO	1st	M20
TELE_FS	1st	L20
TELE_INT	1st	K21
TELE_RESET	1st	K22
TELE_RINGIN1	1st	M21
TELE_RINGIN2	1st	M22
TELE_RINGIN3	1st	L21
TELE_RINGIN4	1st	L22
TEST	1st	F4
UART_CTS	1st	B3
UART_RTS	1st	A3
UART_RX	1st	B4
UART_TX	1st	C4

Terminal (Part 8 of 10)		
Name	**Fn[1]**	**No.**
VDD	1st	AB6
VDD	1st	J10
VDD	1st	J11
VDD	1st	J12
VDD	1st	J13
VDD	1st	K14
VDD	1st	K9
VDD	1st	L14
VDD	1st	L9
VDD	1st	M14
VDD	1st	M9
VDD	1st	N14
VDD	1st	N9
VDD	1st	P10
VDD	1st	P11
VDD	1st	P12
VDD	1st	P13
VDD_PLL	1st	N19
VDDA_AIC	1st	R4
VDDA_AIC	1st	T4
VDDA_AIC	1st	W7
VDDA_AIC	1st	W8
VDDA_PHY0_1	1st	U21
VDDA_PHY0_2	1st	U20
VDDA_PHY0_34	1st	Y20
VDDA_PHY1_1	1st	U22
VDDA_PHY1_2	1st	U19
VDDA_PHY1_34	1st	P20
VDDS	1st	D10
VDDS	1st	D13
VDDS	1st	D14
VDDS	1st	D15
VDDS	1st	D16
VDDS	1st	D7
VDDS	1st	D8
VDDS	1st	D9
VDDS	1st	G19
VDDS	1st	G4
VDDS	1st	H19
VDDS	1st	H4
VDDS	1st	J19

Terminal (Part 9 of 10)		
Name	**Fn[1]**	**No.**
VDDS	1st	J4
VDDS	1st	K19
VDDS	1st	K4
VDDS	1st	N4
VDDS	1st	P4
VDDS	1st	W10
VDDS	1st	W13
VDDS	1st	W14
VDDS	1st	W15
VDDS	1st	W16
VDDS	1st	W9
VLYNQ5_CLK	1st	K3
VLYNQ5_RX_D0	1st	K2
VLYNQ5_RX_D1	1st	K1
VLYNQ5_TX_D0	1st	L2
VLYNQ5_TX_D1	1st	L1
VR_BASE2	1st	R2
VR_BASE3	1st	Y22
VR_ENBL	1st	AA6
VSS	1st	A1
VSS	1st	A2
VSS	1st	A21
VSS	1st	A22
VSS	1st	B1
VSS	1st	B2
VSS	1st	B21
VSS	1st	B22
VSS	1st	C20
VSS	1st	C3
VSS	1st	D19
VSS	1st	D4
VSS	1st	J14
VSS	1st	J9
VSS	1st	K10
VSS	1st	K11
VSS	1st	K12
VSS	1st	K13
VSS	1st	L10
VSS	1st	L11
VSS	1st	L12
VSS	1st	L13

Terminal (Part 10 of 10)		
Name	**Fn[1]**	**No.**
VSS	1st	M10
VSS	1st	M11
VSS	1st	M12
VSS	1st	M13
VSS	1st	N10
VSS	1st	N11
VSS	1st	N12
VSS	1st	N13
VSS_AIC	1st	AA1
VSS_AIC	1st	AA2
VSS_AIC	1st	AB1
VSS_AIC	1st	AB2
VSS_AIC	1st	W4
VSS_AIC	1st	Y3
VSS_AIC_CLK	1st	P9
VSS_PHY0_1	1st	V21
VSS_PHY0_1	1st	W21
VSS_PHY0_2	1st	V20
VSS_PHY0_34	1st	W20
VSS_PHY0_ESD	1st	V19
VSS_PHY1_1	1st	R21
VSS_PHY1_1	1st	T21
VSS_PHY1_2	1st	T20
VSS_PHY1_34	1st	R20
VSS_PHY1_ESD	1st	T19
VSS_PLL	1st	P14
VSS_REF_CLK	1st	N21

[1] Package terminals may have primary functions (1st), secondary functions (2nd), and/or tertiary functions (3rd).

Table 3-3 Terminal Assignments by Terminal Number[1] (Part 1 of 9)

Terminal No.	Primary		Secondary		Tertiary		Pull Up/Down	Drive Current (mA)	Fail Safe	Low Noise	Other
	Signal Name	Type	Signal Name	Type	Signal Name	Type					
A1	VSS	G									GND
A2	VSS	G									GND
A3	UART_RTS	O						4			
A4	$\overline{\text{EM\_WE}}$	O						8			
A5	$\overline{\text{EM\_CAS}}$	O						8			
A6	EM_RAS	O						8			
A7	$\overline{\text{EM\_CS5}}$	O						8			
A8	$\overline{\text{EM\_CS2}}$	O						8			
A9	$\overline{\text{EM\_WE\_DQM3}}$	O						8			
A10	EM_D30	I/O					u	8			
A11	EM_D28	I/O					u	8			
A12	EM_D24	I/O					u	8			
A13	EM_D20	I/O					u	8			
A14	EM_D17	I/O					u	8			
A15	EM_D14	I/O					u	8			
A16	EM_D11	I/O					u	8			
A17	EM_D08	I/O					u	8			
A18	EM_D04	I/O					u	8			
A19	EM_D01	I/O					u	8			
A20	EM_A23	I/O					u	8			
A21	VSS	G									GND
A22	VSS	G									GND
AA1	VSS_AIC	G									GND analog
AA2	VSS_AIC	G									GND analog
AA3	AIC_HAND_P	I									analog
AA4	AIC_HAND_M	I									analog
AA5	AIC_MIC_P	I									analog
AA6	$\overline{\text{VR\_ENBL}}$	I									analog
AA7	KEYPAD01	I/O			GPIO09	I/O	D	4	FS	LN	
AA8	KEYPAD03	I/O			GPIO11	I/O	D	4	FS	LN	
AA9	KEYPAD06	I/O			GPIO14	I/O	D	4	FS	LN	
AA10	KEYPAD09	I/O			GPIO17	I/O	U	4		LN	
AA11	KEYPAD12	I/O			GPIO20	I/O	U	4		LN	
AA12	LCD_BIAS_E0	I/O	$\overline{\text{AIC\_RESET}}$	I			U	4			
AA13	LCD_VSYNC_A	I/O	MII_MD_CLK	I/O			U	4			
AA14	LCD_D02	I/O	MII_P0_TX_D1	O	GPIO26	I/O	U	4			
AA15	LCD_D05	I/O	MII_P0_TX_ENBL	O	GPIO29	I/O	U	4			
AA16	LCD_D08	I/O	MII_P0_COL	I	GPIO32	I/O	U	4			
AA17	LCD_D11	I/O	MII_P0_RX_DV	I	GPIO35	I/O	U	4			

Table 3-3 Terminal Assignments by Terminal Number[1] (Part 2 of 9)

Terminal No.	Primary		Secondary		Tertiary		Pull Up/Down	Drive Current (mA)	Fail Safe	Low Noise	Other
	Signal Name	Type	Signal Name	Type	Signal Name	Type					
AA18	LCD_D15	I/O	MII_P0_RX_D3	I	GPIO39	I/O	U	4			
AA19	$\overline{\text{P0\_LINK}}$	I/O	AIC_DI	I	P0_FX_RX	I	U	8			
AA20	$\overline{\text{P0\_FDUPLEX}}$	I/O	AIC_S_CLK	O	P0_FX_ENBL	O	U	8			
AA21	N/C										
AA22	N/C										
AB1	VSS_AIC	G									GND analog
AB2	VSS_AIC	G									GND analog
AB3	AIC_CALL_P	I									analog
AB4	AIC_CALL_M	I									analog
AB5	AIC_MIC_M	I									analog
AB6	VDD	O									1.5 V core
AB7	KEYPAD00	I/O			GPIO08	I/O	D	4	FS	LN	
AB8	KEYPAD02	I/O			GPIO10	I/O	D	4	FS	LN	
AB9	KEYPAD05	I/O			GPIO13	I/O	D	4	FS	LN	
AB10	KEYPAD08	I/O			GPIO16	I/O	U	4		LN	
AB11	KEYPAD11	I/O			GPIO19	I/O	U	4		LN	
AB12	KEYPAD15	I/O			GPIO23	I/O	U	4		LN	
AB13	LCD_E1	I/O	DSP_FUNCTEST1	I/O			U	8			
AB14	LCD_D01	I/O	MII_P0_TX_D0	O	GPIO25	I/O	U	4			
AB15	LCD_D04	I/O	MII_P0_TX_D3	O	GPIO28	I/O	U	4			
AB16	LCD_D07	I/O	MII_P0_LINK	I	GPIO31	I/O	U	4			
AB17	LCD_D10	I/O	MII_P0_RX_CLK	I	GPIO34	I/O	U	4			
AB18	LCD_D14	I/O	MII_P0_RX_D2	I	GPIO38	I/O	U	4			
AB19	$\overline{\text{P0\_100MB}}$	I/O	AIC_DO	O	P0_FX_SD	I	U	8	FS	LN	
AB20	$\overline{\text{P0\_ACTIVITY}}$	I/O	AIC_FS	O	P0_FX_TX	O	U	8			
AB21			$\overline{\text{AIC\_PWRDWN}}$	I			U	8			
AB22	N/C										
B1	VSS	G									GND
B2	VSS	G									GND
B3	UART_CTS	I					U				
B4	UART_RX	I					U				
B5	$\overline{\text{EM\_OE}}$	O						8			
B6	EM_WAIT	I					D				
B7	$\overline{\text{EM\_CS4}}$	O						8			
B8	$\overline{\text{EM\_CS1}}$	O						8			
B9	$\overline{\text{EM\_WE\_DQM2}}$	O						8			
B10	EM_D31	I/O					u	8			
B11	EM_D29	I/O					u	8			
B12	EM_D25	I/O					u	8			

Table 3-3 Terminal Assignments by Terminal Number[1] (Part 3 of 9)

Terminal No.	Primary		Secondary		Tertiary		Pull Up/Down	Drive Current (mA)	Fail Safe	Low Noise	Other
	Signal Name	Type	Signal Name	Type	Signal Name	Type					
B13	EM_D21	I/O					u	8			
B14	EM_D18	I/O					u	8			
B15	EM_D15	I/O					u	8			
B16	EM_D12	I/O					u	8			
B17	EM_D09	I/O					u	8			
B18	EM_D05	I/O					u	8			
B19	EM_D00	I/O					u	8			
B20	EM_A22	I/O					u	8			
B21	VSS	G									GND
B22	VSS	G									GND
C1	$\overline{\text{RESET\_I}}$	I							FS		
C2	$\overline{\text{RESET\_O}}$	O						4	FS	LN	
C3	VSS	G									GND
C4	UART_TX	O						4			
C5	EM_RW	O						8			
C6	EM_HIZ	I					D				
C7	$\overline{\text{EM\_CS3}}$	O						8			
C8	$\overline{\text{EM\_CS0}}$	O						8			
C9	$\overline{\text{EM\_WE\_DQM1}}$	O						8			
C10	$\overline{\text{EM\_WE\_DQM0}}$	O						8			
C11	EM_D27	I/O					u	8			
C12	EM_D23	I/O					u	8			
C13	EM_D19	I/O					u	8			
C14	EM_D16	I/O					u	8			
C15	EM_D13	I/O					u	8			
C16	EM_D10	I/O					u	8			
C17	EM_D07	I/O					u	8			
C18	EM_D03	I/O					u	8			
C19	EM_A21	I/O					u	8			
C20	VSS	G									GND
C21	EM_A20	I/O					u	8			
C22	EM_A19	I/O					u	8			
D1	SSP1	I/O					D	4		LN	
D2	SSP2	I/O					D	4		LN	
D3	SSP0	I/O					D	4		LN	
D4	VSS	G									GND
D5	EM_CKE	O						8			
D6	EM_CLK	I/O						8			
D7	VDDS	P									3.3-V I/O

Table 3-3 Terminal Assignments by Terminal Number[1] (Part 4 of 9)

Terminal No.	Primary		Secondary		Tertiary		Pull Up/Down	Drive Current (mA)	Fail Safe	Low Noise	Other
	Signal Name	Type	Signal Name	Type	Signal Name	Type					
D8	VDDS	P									3.3-V I/O
D9	VDDS	P									3.3-V I/O
D10	VDDS	P									3.3-V I/O
D11	EM_D26	I/O					u	8			
D12	EM_D22	I/O					u	8			
D13	VDDS	P									3.3-V I/O
D14	VDDS	P									3.3-V I/O
D15	VDDS	P									3.3-V I/O
D16	VDDS	P									3.3-V I/O
D17	EM_D06	I/O					u	8			
D18	EM_D02	I/O					u	8			
D19	VSS	G									GND
D20	EM_A18	I/O					u	8			
D21	EM_A17	I/O					u	8			
D22	EM_A16	I/O					u	8			
E1	$\overline{\text{EJTAG\_TRST1}}$	I					D		FS		
E2	$\overline{\text{EJTAG\_SYSRST}}$	I					U				
E3	EJTAG_DINT	I					U				
E4	SSP3	I/O					D	4		LN	
E19	EM_A15	I/O					u	8			
E20	EM_A14	I/O					u	8			
E21	EM_A13	I/O					u	8			
E22	EM_A12	I/O					u	8			
F1	EJTAG_TDO	O						4	FS	LN	
F2	EJTAG_TCK	I					U				
F3	$\overline{\text{EJTAG\_TRST0}}$	I					D		FS		
F4	TEST	I					D		FS		
F19	EM_A11	I/O					u	8			
F20	EM_A10	I/O					u	8			
F21	EM_A09	I/O					u	8			
F22	EM_A08	I/O					u	8			
G1	JTAG_EMU1	I/O					U	4		LN	
G2	EJTAG_TMS	I					U				
G3	EJTAG_TDI	I					U				
G4	VDDS	P									3.3-V I/O
G19	VDDS	P									3.3-V I/O
G20	EM_A07	I/O					u	8			
G21	EM_A06	I/O					u	8			
G22	EM_A05	I/O					u	8			

Table 3-3 Terminal Assignments by Terminal Number[1] (Part 5 of 9)

Terminal No.	Primary		Secondary		Tertiary		Pull Up/Down	Drive Current (mA)	Fail Safe	Low Noise	Other
	Signal Name	Type	Signal Name	Type	Signal Name	Type					
H1	JTAG_TDI	I					U				
H2	$\overline{\text{JTAG\_TRST}}$	I					D		FS		
H3	JTAG_EMU0	I/O					U	4		LN	
H4	VDDS	P									3.3-V I/O
H19	VDDS	P									3.3-V I/O
H20	EM_A04	I/O					u	8			
H21	EM_A03	I/O					u	8			
H22	EM_A02	I/O					u	8			
J1	JTAG_TMS	I					U				
J2	JTAG_TDO	O						4	FS	LN	
J3	JTAG_TCK	I					U				
J4	VDDS	P									3.3-V I/O
J9	VSS	G									GND
J10	VDD	P									1.5-V core
J11	VDD	P									1.5-V core
J12	VDD	P									1.5-V core
J13	VDD	P									1.5-V core
J14	VSS	G									GND
J19	VDDS	P									3.3-V I/O
J20	EM_A01	I/O					u	8			
J21	EM_A00	I/O					u	8			
J22	TELE_CLK_O	I/O					U	4			
K1	VLYNQ5_RX_D1	I									
K2	VLYNQ5_RX_D0	I									
K3	VLYNQ5_CLK	I/O					U	8			
K4	VDDS	P									3.3-V I/O
K9	VDD	P									1.5-V core
K10	VSS	G									GND
K11	VSS	G									GND
K12	VSS	G									GND
K13	VSS	G									GND
K14	VDD	P									1.5-V core
K19	VDDS	P									3.3-V I/O
K20	$\overline{\text{TELE\_CS}}$	I/O			GPIO49	I/O	U	4			
K21	TELE_INT	I/O			GPIO50	I/O	U	4			
K22	$\overline{\text{TELE\_RESET}}$	I/O			GPIO51	I/O	U	4			
L1	VLYNQ5_TX_D1	I/O						8			
L2	VLYNQ5_TX_D0	I/O						8			
L3	N/C										

Table 3-3 Terminal Assignments by Terminal Number[1] (Part 6 of 9)

Terminal No.	Primary		Secondary		Tertiary		Pull Up/Down	Drive Current (mA)	Fail Safe	Low Noise	Other
	Signal Name	Type	Signal Name	Type	Signal Name	Type					
L4	N/C										
L9	VDD	P									1.5-V core
L10	VSS	G									GND
L11	VSS	G									GND
L12	VSS	G									GND
L13	VSS	G									GND
L14	VDD	P									1.5-V core
L19	TELE_CLK_I	I/O			GPIO43	I/O	U	4			
L20	TELE_FS	I/O			GPIO48	I/O	U	4			
L21	TELE_RINGIN3	I/O			GPIO46	I/O	U	4			
L22	TELE_RINGIN4	I/O			GPIO47	I/O	U	4			
M1	N/C										
M2	N/C										
M3	McBSP_CLK_RX	I/O					U	4		LN	
M4	N/C										
M9	VDD	P									1.5-V core
M10	VSS	G									GND
M11	VSS	G									GND
M12	VSS	G									GND
M13	VSS	G									GND
M14	VDD	P									1.5-V core
M19	TELE_DCLK	I/O			GPIO40	I/O	U	4			
M20	TELE_DO	I/O			GPIO42	I/O	U	4			
M21	TELE_RINGIN1	I/O			GPIO44	I/O	U	4			
M22	TELE_RINGIN2	I/O			GPIO45	I/O	U	4			
N1	N/C										
N2	McBSP_CLK_TX	I/O					U	4		LN	
N3	McBSP_D_RX	I					D		FS		
N4	VDDS	P									3.3-V I/O
N9	VDD	P									1.5-V core
N10	VSS	G									GND
N11	VSS	G									GND
N12	VSS	G									GND
N13	VSS	G									GND
N14	VDD	P									1.5-V core
N19	VDD_PLL	P									V analog
N20	TELE_DI	I/O			GPIO41	I/O	U	4			
N21	VSS_REF_CLK	G									GND analog
N22	REF_CLK_O	O									oscillator

Table 3-3 Terminal Assignments by Terminal Number[1] (Part 7 of 9)

Terminal No.	Primary		Secondary		Tertiary		Pull Up/Down	Drive Current (mA)	Fail Safe	Low Noise	Other
	Signal Name	Type	Signal Name	Type	Signal Name	Type					
P1	McBSP_D_TX	O						4	FS	LN	
P2	McBSP_FS_RX	I/O					D	4	FS	LN	
P3	McBSP_FS_TX	I/O					D	4	FS	LN	
P4	VDDS	P									3.3-V I/O
P9	VSS_AIC_CLK	G									GND analog
P10	VDD	P									1.5-V core
P11	VDD	P									1.5-V core
P12	VDD	P									1.5-V core
P13	VDD	P									1.5-V core
P14	VSS_PLL	G									GND analog
P19	N/C										
P20	VDDA_PHY1_34	P									V analog
P21	ALT_CLK_I	I					D				
P22	REF_CLK_I	I/O									oscillator
R1	AIC_CLK_I	I/O									oscillator
R2	VR_BASE2	O									V regulator
R3	GPIO00	I/O			EXT_INT1	I	U	4		LN	
R4	VDDA_AIC	P									V analog
R19	N/C										
R20	VSS_PHY1_34	G									GND analog
R21	VSS_PHY1_1	G									GND analog
R22	N/C										
T1	AIC_CLK_O	O									oscillator
T2	GPIO03	I/O			EXT_INT4	I	U	4		LN	
T3	GPIO01	I/O			EXT_INT2	I	U	4		LN	
T4	VDDA_AIC	P									V analog
T19	VSS_PHY1_ESD	G									GND analog
T20	VSS_PHY1_2	G									GND analog
T21	VSS_PHY1_1	G									GND analog
T22	N/C										
U1	GPIO06	I/O					U	4		LN	
U2	GPIO04	I/O					U	4		LN	
U3	GPIO02	I/O			EXT_INT3	I	U	4		LN	
U4	AIC_150_M2	O									analog
U19	VDDA_PHY1_2	P									V analog
U20	VDDA_PHY0_2	P									V analog
U21	VDDA_PHY0_1	P									V analog
U22	VDDA_PHY1_1	P									V analog
V1	GPIO07	I/O					U	4		LN	

Table 3-3 Terminal Assignments by Terminal Number[1] (Part 8 of 9)

Terminal No.	Primary		Secondary		Tertiary		Pull Up/Down	Drive Current (mA)	Fail Safe	Low Noise	Other
	Signal Name	Type	Signal Name	Type	Signal Name	Type					
V2	GPIO05	I/O			SSP4	I/O	U	4		LN	
V3	AIC_150_P1	O									analog
V4	AIC_150_P2	O									analog
V19	VSS_PHY0_ESD	G									GND analog
V20	VSS_PHY0_2	G									GND analog
V21	VSS_PHY0_1	G									GND analog
V22	P0_TX_M	O									analog
W1	AIC_600_P	O									analog
W2	AIC_LINE_P	I									analog
W3	AIC_150_M1	O									analog
W4	VSS_AIC	G									GND analog
W5	AIC_8_M	O									analog
W6	AIC_8_P	O									analog
W7	VDDA_AIC	P									V analog
W8	VDDA_AIC	P									V analog
W9	VDDS	P									3.3-V I/O
W10	VDDS	P									3.3-V I/O
W11	KEYPAD13	I/O			GPIO21	I/O	U	4		LN	
W12	$\overline{\text{LCD\_HSYNC\_W}}$	I/O	MII_MD_IO	I/O			U	4			
W13	VDDS	P									3.3-V I/O
W14	VDDS	P									3.3-V I/O
W15	VDDS	P									3.3-V I/O
W16	VDDS	P									3.3-V I/O
W17	LCD_D13	I/O	MII_P0_RX_D1	I	GPIO37	I/O	U	4			
W18	PHY_REF	O									analog
W19	P0_RX_M	I									analog
W20	VSS_PHY0_34	G									GND analog
W21	VSS_PHY0_1	G									GND analog
W22	P0_TX_P	O									analog
Y1	AIC_600_M	O									analog
Y2	AIC_LINE_M	I									analog
Y3	VSS_AIC	G									GND analog
Y4	AIC_HEAD_P	I									analog
Y5	AIC_HEAD_M	I									analog
Y6	AIC_MIC_BIAS	O									analog
Y7	AIC_DAC_6BIT	O									analog
Y8	KEYPAD04	I/O			GPIO12	I/O	D	4	FS	LN	
Y9	KEYPAD07	I/O			GPIO15	I/O	D	4	FS	LN	
Y10	KEYPAD10	I/O			GPIO18	I/O	U	4		LN	

Table 3-3 Terminal Assignments by Terminal Number[1] (Part 9 of 9)

Terminal No.	Primary		Secondary		Tertiary		Pull Up/Down	Drive Current (mA)	Fail Safe	Low Noise	Other
	Signal Name	Type	Signal Name	Type	Signal Name	Type					
Y11	KEYPAD14	I/O			GPIO22	I/O	U	4		LN	
Y12	LCD_PIXEL_STRB	I/O	DSP_FUNCTEST0	I/O			U	8			
Y13	LCD_D00	I/O	MII_P0_CRS	I	GPIO24	I/O	U	4			
Y14	LCD_D03	I/O	MII_P0_TX_D2	O	GPIO27	I/O	U	4			
Y15	LCD_D06	I/O	MII_P0_TX_CLK	I	GPIO30	I/O	U	4			
Y16	LCD_D09	I/O	MII_P0_RX_ERR	I	GPIO33	I/O	U	4			
Y17	LCD_D12	I/O	MII_P0_RX_D0	I	GPIO36	I/O	U	4			
Y18	PHY_REF_RTN	I									analog
Y19	P0_RX_P	I									analog
Y20	VDDA_PHY0_34	P									V analog
Y21	PHY_TEST	I									analog
Y22	VR_BASE3	O									V regulator
End of Table 3-3											

[1] See Table 3-1for functional symbol definitions.

3.3 Signal Descriptions

Because useful I/O signals are multiplexed over the primary I/O signals, three columns are provided in the following tables. The columns are defined as 1st for the primary I/O signals, 2nd for the secondary I/O signals, and 3rd for the tertiary I/O signals. Signals of interest that are described in each table are highlighted in **bold** text.

Due to the multiplexing capabilities of several of the TNETV1056 I/O terminals, certain Type terminal definitions may not accurately define the input or output designation of a particular signal. In these special cases, the correct input designation is defined as (IN), while the correct output designation is defined as (OUT) in the Description field.

3.3.1 External Memory Interface (EMIF)

The EMIF provides glueless connectivity to the following memory device types (see Table 3-4 through Table 3-6):

- Synchronous DRAM (SDRAM)
- Asynchronous memory (includes flash, ROM, or RAM)
- Host-port interface (HPI), a memory-mapped registered interface to standard TI DSP subsystems utilizing asynchronous memory (flash, ROM, or RAM)

3.3.1.1 Address Bus

Table 3-4 EMIF Address I/Os

Terminal No.	Type	1st	2nd	3rd	Description
J21	I/O	**EM_A00**			EMIF address bus (OUT). This bus (EM_A[23:00]) provides an address when accessing the EMIF. The function of EM_A[23:21] changes dependent on the data bus width of the external device (detailed in the *TNETV1050 User's Guide*) . Boot configuration (IN). This bus (EM_A[23:00]) is sampled at $\overline{\text{RESET\_I}}$ deactivation. The information sampled determines certain boot configuration modes (for more information, see section 3.4 "Boot Configuration" on page 60).
J20		**EM_A01**			
H22		**EM_A02**			
H21		**EM_A03**			
H20		**EM_A04**			
G22		**EM_A05**			
G21		**EM_A06**			
G20		**EM_A07**			
F22		**EM_A08**			
F21		**EM_A09**			
F20		**EM_A10**			
F19		**EM_A11**			
E22		**EM_A12**			
E21		**EM_A13**			
E20		**EM_A14**			
E19		**EM_A15**			
D22		**EM_A16**			
D21		**EM_A17**			
D20		**EM_A18**			
C22		**EM_A19**			
C21		**EM_A20**			
C19		**EM_A21**			
B20		**EM_A22**			
A20		**EM_A23**			
End of Table 3-4					

3.3.1.2 Data Bus

Table 3-5 EMIF Data I/Os

Terminal No.	Type	1st	2nd	3rd	Description
B19	I/O	**EM_D00**			EMIF data bus. This bus (EM_D[31:00]) provides the data path when accessing the EMIF. Valid external data bus widths include 32 bit, 16 bit, and 8 bit (for asynchronous only).
A19		**EM_D01**			
D18		**EM_D02**			
C18		**EM_D03**			
A18		**EM_D04**			
B18		**EM_D05**			
D17		**EM_D06**			
C17		**EM_D07**			
A17		**EM_D08**			
B17		**EM_D09**			
C16		**EM_D10**			
A16		**EM_D11**			
B16		**EM_D12**			
C15		**EM_D13**			
A15		**EM_D14**			
B15		**EM_D15**			
C14		**EM_D16**			
A14		**EM_D17**			
B14		**EM_D18**			
C13		**EM_D19**			
A13		**EM_D20**			
B13		**EM_D21**			
D12		**EM_D22**			
C12		**EM_D23**			
A12		**EM_D24**			
B12		**EM_D25**			
D11		**EM_D26**			
C11		**EM_D27**			
A11		**EM_D28**			
B11		**EM_D29**			
A10		**EM_D30**			
B10		**EM_D31**			
End of Table 3-5					

3.3.1.3 Control Signals

Table 3-6 EMIF Control I/Os

Terminal No.	Type	1st	2nd	3rd	Description
C8	O	**EM_CS0**			EMIF chip select 0. Designated for asynchronous memory (flash) accesses (32M-byte addressability).
B8	O	**EM_CS1**			EMIF chip select 1. Designated for SDRAM accesses (64M-byte addressability).
A8	O	**EM_CS2**			EMIF chip select 2. Designated for SDRAM accesses (64M-byte addressability).
C7	O	**EM_CS3**			EMIF chip select 3. Designated for asynchronous memory accesses (16M-byte addressability).
B7	O	**EM_CS4**			EMIF chip select 4. Designated for asynchronous memory accesses (16M-byte addressability).
A7	O	**EM_CS5**			EMIF chip select 5. Designated for asynchronous memory accesses (16M-byte addressability).
D6	I/O	**EM_CLK**			SDRAM clock (OUT)
A6	O	**EM_RAS**			SDRAM row address strobe
A5	O	**EM_CAS**			SDRAM column address strobe
A4	O	**EM_WE**			SDRAM write enable control. Asynchronous memory write strobe control.
D5	O	**EM_CKE**			SDRAM clock enable
C10	O	**EM_WE_DQM0**			SDRAM ($\overline{DQM}$): Data byte masked when this control signal is sampled high for either reads or writes. The data byte is read or written when sampled low. Asynchronous memory ($\overline{WE}$): Write strobe control. In addition, may be used as read-mode byte enable through register program control.
C9	O	**EM_WE_DQM1**			
B9	O	**EM_WE_DQM2**			
A9	O	**EM_WE_DQM3**			
B5	O	**EM_OE**			Asynchronous memory read strobe control
C5	O	**EM_R/W**			Asynchronous memory read or write enable control
B6	I	**EM_WAIT**			External device wait state control during asynchronous memory accesses. Must be register bit enabled to become effective and can be positive or negative active.
C6	I	**EM_HIZ**			EMIF 3-state control. For test purposes only. Must be held low (with internal pulldown) for normal operation.
End of Table 3-6					

3.3.2 Ethernet

The TNETV1056 provides one Ethernet port, referred to as Port 0 (P0). This port provides the following I/O options:

- Fully integrated IEEE Std 802.3/802.3u-compatible 10-Mbps/100-Mbps Ethernet PHY
- Optional IEEE Std 802.3 media independent interface (MII) port capable of operating up to 30 external PHY devices. Reverse MII, reduced MII (RMII), and serial MII (SMII) modes of operation are not supported. Each MII can accommodate the following operational options:
  - Internal PHY mode. The external MII port is inactive.
  - Internal PHY mode with MII observation. This test mode allows external visibility of the information passed between the internal MAC and the internal PHY on the MII.
  - Internal PHY disabled. The internal PHY is disabled and the MII is being driven by the MAC in order to control an external PHY.
- Internal PHY LED status control outputs

3.3.2.1 Management MII

This two-terminal serial interface provides register programmability to any PHY attached to the TNETV1056 as defined in the following:

- The TNETV1056 can provide register control to external PHY devices (up to 30).
- External controllers can provide register control of the internal TNETV1056 PHY.

Table 3-7 Management Data MII I/Os

Terminal No.	Type	1st	2nd	3rd	Description
W12	I/O	$\overline{\text{LCD\_HSYNC\_W}}$	**MII_MD_IO**		Serial management data stream for PHY register control
AA13	I/O	LCD_VSYNC_A	**MII_MD_CLK**		Serial management clock that synchronizes the MII_MD_IO
End of Table 3-7					

3.3.2.2 Analog PHY

Table 3-8 Analog PHY I/Os

Terminal No.	Type	1st	2nd	3rd	Description
W18	O	**PHY_REF**			A 12.4-kΩ 1% resistor is connected between these two I/O terminals.
Y18	I	**PHY_REF_RTN**			
End of Table 3-8					

3.3.2.3 Port 0 PHY

Table 3-9 Port 0 PHY I/Os

Terminal No.	Type	1st	2nd	3rd	Description
W19	I	**P0_RX_M**			Port 0 differential receiver +/– pair, to magnetics. If this Ethernet PHY is not used, tie both terminals to ground.
Y19		**P0_RX_P**			
V22	O	**P0_TX_M**			Port 0 differential transmit +/– pair, to magnetics
W22		**P0_TX_P**			
AB19	I/O	**$\overline{\text{P0\_100MB}}$**	AIC_DO	**P0_FX_SD**	$\overline{\text{P0\_100MB}}$ (OUT) LED 1, low = 100 Mbps, high = 10 Mbps P0_FX_SD (IN) 100 Base-FX signal detect indicating a valid received signal from the external FX transceiver
AA19	I/O	**$\overline{\text{P0\_LINK}}$**	AIC_DI	**P0_FX_RX**	$\overline{\text{P0\_LINK}}$ (OUT) LED 2, low = port 0 link established with the internal PHY P0_FX_RX (IN) 100 Base-FX receiver data
AB20	I/O	**$\overline{\text{P0\_ACTIVITY}}$**	AIC_FS	**P0_FX_TX**	$\overline{\text{P0\_ACTIVITY}}$ (OUT) LED 3, low = carrier sense activity P0_FX_TX (OUT) 100 Base-FX transmit data
AA20	I/O	**$\overline{\text{P0\_FDUPLEX}}$**	AIC_S_CLK	**P0_FX_ENBL**	$\overline{\text{P0\_FDUPLEX}}$ (OUT) LED 4, low = full duplex, high = half duplex P0_FX_ENBL (OUT) Enable the external FX-compatible driver for P0_FX_TX
End of Table 3-9					

3.3.2.4 Port 0 MII

Table 3-10 Port 0 MII I/Os

Terminal No.	Type	1st	2nd	3rd	Description
AA15	I/O	LCD_D05	**MII_P0_TX_ENBL**	GPIO29	Port 0 MII transmit enable (OUT)
Y15	I/O	LCD_D06	**MII_P0_TX_CLK**	GPIO30	Port 0 MII transmit clock (IN)
AB14	I/O	LCD_D01	**MII_P0_TX_D0**	GPIO25	Port 0 MII transmit data nibble (OUT). Data is synchronous with MII_P0_TX_CLK. Data is valid when MII_P0_TX_ENBL is active.
AA14		LCD_D02	**MII_P0_TX_D1**	GPIO26	
Y14		LCD_D03	**MII_P0_TX_D2**	GPIO27	
AB15		LCD_D04	**MII_P0_TX_D3**	GPIO28	
AB17	I/O	LCD_D10	**MII_P0_RX_CLK**	GPIO34	Port 0 MII receiver clock (IN)
Y17	I/O	LCD_D12	**MII_P0_RX_D0**	GPIO36	Port 0 MII receiver data nibble. (IN). Data is synchronous with MII_P0_RX_CLK. Data is valid when MII_P0_RX_DV is active.
W17		LCD_D13	**MII_P0_RX_D1**	GPIO37	
AB18		LCD_D14	**MII_P0_RX_D2**	GPIO38	
AA18		LCD_D15	**MII_P0_RX_D3**	GPIO39	
AA17	I/O	LCD_D11	**MII_P0_RX_DV**	GPIO35	Port 0 MII receiver data valid (IN)
Y16	I/O	LCD_D09	**MII_P0_RX_ERR**	GPIO33	Port 0 MII receiver data coding error (IN)
Y13	I/O	LCD_D00	**MII_P0_CRS**	GPIO24	Port 0 MII carrier sense (IN). A frame carrier signal is being received.
AA16	I/O	LCD_D08	**MII_P0_COL**	GPIO32	Port 0 MII collision sense (IN). In half-duplex mode, indicates network collision. In full-duplex mode, transmission of new frames does not commence.
AB16	I/O	LCD_D07	**MII_P0_LINK**	GPIO31	Port 0 MII link active (IN). The external PHY activates this signal when a link is established.
End of Table 3-10					

3.3.3 Voice Codec Interface

The on-chip voice codec is a mixed-signal dual-channel voice codec. Featuring two analog-to-digital converter (ADCs) and two digital-to-analog converters (DACs) that can interface to a handset, headset, speaker, microphone, or subscriber line through a programmable analog crosspoint.

Table 3-11 Voice Codec I/Os (Part 1 of 2)

Terminal No.	Type	1st	2nd	3rd	Description
W3	O	**AIC_150_M1**			Inverting headset output. This terminal along with the AIC_150_P1 terminal forms the differential output capable of driving a 150-Ω load.
V3		**AIC_150_P1**			Non-inverting headset output. This terminal along with the AIC_150_M1 terminal forms the differential output capable of driving a 150-Ω load.
U4	O	**AIC_150_M2**			Inverting handset output. This terminal along with the AIC_150_P2 terminal forms the differential output capable of driving a 150-Ω load.
V4		**AIC_150_P2**			Non-inverting handset output. This terminal along with the AIC_150_M2 terminal forms the differential output capable of driving a 150-Ω load.
Y1	O	**AIC_600_M**			Inverting line output. This terminal along with the AIC_600_P terminal forms the differential output capable of driving a 600-Ω load.
W1		**AIC_600_P**			Non-inverting line output. This terminal along with the AIC_600_M terminal forms the differential output capable of driving a 600-Ω load.
W5	O	**AIC_8_M**			Inverting analog output from speaker amplifier. This terminal along with AIC_8_M forms the differential output cabable of driving an 8-Ω speaker.
W6		**AIC_8_P**			Non-inverting analog output from speaker amplifier. This terminal along with AIC_8_P forms the differential output cabable of driving an 8-Ω speaker.
AB4	I	**AIC_CALL_M**			Caller ID amplifier analog inverting input.
AB3		**AIC_CALL_P**			Caller ID amplifier analog non-inverting input.
AA4	I	**AIC_HAND_M**			Handset amplifier analog inverting input.
AA3		**AIC_HAND_P**			Handset amplifier analog non-inverting input.
Y5	I	**AIC_HEAD_M**			Headset amplifier analog inverting input.
Y4		**AIC_HEAD_P**			Headset amplifier analog non-inverting input.
Y2	I	**AIC_LINE_M**			Line interface amplifier analog inverting input.
W2		**AIC_LINE_P**			Line interface amplifier analog non-inverting input.
AB5	I	**AIC_MIC_M**			Microphone amplifier analog inverting input.
AA5		**AIC_MIC_P**			Microphone amplifier analog non-inverting input.
Y6	O	**AIC_MIC_BIAS**			Microphone analog output bias voltage for handset, headset, and microphone analog inputs.
Y7	O	**AIC_DAC_6BIT**			6-bit DAC output voltage, which may be used to drive an LCD display.
R1	I/O	**AIC_CLK_I**			Differential crystal pair for the voice codec clock. The recommended frequency is 8.1920 MHz.
T1	O	**AIC_CLK_O**			
AA19	I/O	$\overline{\text{P0\_LINK}}$	**AIC_DI**	P0_FX_RX	Voice codec serial port data input for digital registered control of the voice codec.

Table 3-11 Voice Codec I/Os (Part 2 of 2)

Terminal No.	Type	1st	2nd	3rd	Description
AB19	I/O	$\overline{\text{P0\_100MB}}$	**AIC_DO**	P0_FX_SD	Voice codec serial port data output for digital registered control of the voice codec.
AB20	I/O	$\overline{\text{P0\_ACTIVITY}}$	**AIC_FS**	P0_FX_TX	Voice codec serial port frame synchronization output for digital registered control of the voice codec.
AA20	I/O	$\overline{\text{P0\_FDUPLEX}}$	**AIC_S_CLK**	P0_FX_ENBL	Voice codec serial port clock output for digital registered control of the voice codec. Synchronizes the AIC_DI, AIC_DO, and AIC_FS signals.
AA12	I/O	LCD_BIAS_E0	**$\overline{\text{AIC\_RESET}}$**		Voice codec reset input resetting the voice codec when held active for at least six AIC_S_CLK periods.
AB21	I/O		**$\overline{\text{AIC\_PWRDWN}}$**		Voice codec power down input powering down the voice codec when held active synchronous to AIC_S_CLK.
End of Table 3-11					

3.3.4 Multichannel Buffered Serial Port (McBSP) Interface

The McBSP is a standard TI serial interface controller supporting a wide variety of serial configurations through register control. This interface may be used to drive external codec devices in place of, or in addition to, the internal integrated voice codec. In addition, each signal may be programmed as a DSP-directed GPIO.

Table 3-12 McBSP I/Os

Terminal No.	Type	1st	2nd	3rd	Description
M3	B	**McBSP_CLK_RX**			Receiver clock or DSP GPIO. Synchronizes McBSP_D_RX and McBSP_FS_RX. If not used, hold high (with internal pullup).
N3	I	**McBSP_D_RX**			Receiver data or DSP GPIO. If not used, hold low (with internal pulldown).
P2	B	**McBSP_FS_RX**			Receiver frame synchronization or DSP GPIO. If not used, hold low (with internal pulldown).
N2	B	**McBSP_CLK_TX**			Transmitter clock or DSP GPIO. Synchronizes McBSP_D_TX and McBSP_FS_TX. If not used, hold high (with internal pullup).
P1	O	**McBSP_D_TX**			Transmitter data or DSP general-purpose output only
P3	B	**McBSP_FS_TX**			Transmitter frame synchronization or DSP GPIO. If not used, hold low (with internal pulldown).
End of Table 3-12					

3.3.5 Telephony Interface

The telephony interface provides a glueless digital connection to external telephony circuitry implementing voice over packet (VOP) applications such as telephony codecs.

The telephony interface consists of a digital voice data interface and a digital control interface:

- PCM interface: A data PCM data stream generally supplied to/from the on-chip McBSP. In addition, the PCM-related signals of the telephony interface supplement this PCM data stream (TELE_FS, TELE_CLK, TELE_CLK0).
- Control data interface: A serial data path supplied by either the telephony interface signals (defined below) or the McBSP.

Voice circuits may require the following additional digital control signals:

- Interrupt: This incoming interrupt is supplied by the telephony interface signals (see Table 3-13).
- Ring in: These low-frequency clock signals are supplied by the telephony interface signals (see Table 3-13).

Table 3-13 Telephony Interface I/Os

Terminal No.	Type	1st	2nd	3rd	Description
N20	I	**TELE_DI**		GPIO41	Control data interface serial port data input
M20	I/O	**TELE_DO**		GPIO42	Control data interface serial port data output when the serial interface specifies separate input and output data bits. This is a bidirectional signal when the serial interface specifies a single bidirectional data terminal.
K20	O	**TELE_CS**		GPIO49	Control data interface chip select or enable output
M19	O	**TELE_DCLK**		GPIO40	Control data interface clock output. Synchronizes the control data interface signals TELE_DI, TELE_DO, and $\overline{\text{TELE\_CS}}$.
M21	O	**TELE_RINGIN1**		GPIO44	Ring in control driver output. When inactive, they produce a low frequency (~20-Hz programmable) clock output used to drive the ringer control input on certain SLICs. When inactive, these signals are held low. For true 5-V drive capability, an external transistor is required.
M22		**TELE_RINGIN2**		GPIO45	
L21		**TELE_RINGIN3**		GPIO46	
L22		**TELE_RINGIN4**		GPIO47	
K21	I	**TELE_INT**		GPIO50	Telephony interface subsystem interrupt input
K22	O	**$\overline{\text{TELE\_RESET}}$**		GPIO51	Telephony interface subsystem reset output. Activated by $\overline{\text{RESET\_I}}$ and register control in the DSP subsystem.
L20	O	**TELE_FS**		GPIO48	PCM interface frame synchronization output
L19	I	**TELE_CLK_I**		GPIO43	PCM interface clock in input. External clock source for the PCM subsystem. The PCM subsystem may be programmed for internal (½ DSP_CLK) or external clock source.
J22	O	**TELE_CLK_O**			PCM interface clock output
End of Table 3-13					

3.3.6 LCD Interface

The TNETV1056 LCD controller supports glueless attachment to three different external display types: character displays, rasterized graphics displays (16-bit monochrome or color), and micro-interface graphic displays.

- The character display driver may be used to interface to standard HD44780-type displays.
- The rasterized graphics display driver may be used to interface to passive (STN) or active (TFT) displays.
- The micro-interface graphic display driver may be used to interface to 6800 or 8080 interface-type displays.

Table 3-14 LCD I/Os (Part 1 of 2)

Terminal No.	Type	1st	2nd	3rd	Description
AA13	I/O	**LCD_VSYNC_A**	MII_MD_CLK		Character display mode (OUT), register select (RS) Raster display mode (OUT) STN type = frame clock (FP) TFT type = vertical sync (VSYNC) Micro display mode (OUT) 6800 and 8080 type = Data/not address select (A0)
W12	I/O	**$\overline{\text{LCD\_HSYNC\_W}}$**	MII_MD_IO		Character display mode (OUT), read/not write select (R/W) Raster display mode (OUT) STN type = line clock (LP) TFT type = horizontal synchronization (HSYNC) Micro display mode (OUT) 6800 type = read/not write select (R/W) 8080 type = not write strobe (WR)
Y12	I/O	**LCD_PIXEL_STRB**	DSP_FUNCTEST0		Character display mode (OUT), enable strobe (E0), first display Raster display mode (OUT) STN type = pixel clock (CP) TFT type = pixel clock (CLK) Micro-display mode (OUT) 6800 type = enable strobe (E) 8080 type = not read strobe (RD)
AA12	I/O	**LCD_BIAS_E0**	$\overline{\text{AIC\_RESET}}$		Character display mode not used Raster display mode (OUT) STN type = AC bias (M) TFT type = AC bias (ENABLE) Micro display mode (OUT) 6800 and 8080 type = chip select (CS0), first display
AB13	I/O	**LCD_E1**	DSP_FUNCTEST1		Character display mode (OUT), enable strobe (E1), second display Raster display mode not used Micro display mode (OUT) 6800 and 8080 type = chip select (CS1), second display or clock when programmed for synchronous mode

Table 3-14 LCD I/Os (Part 2 of 2)

Terminal No.	Type	1st	2nd	3rd	Description
Y13	I/O	**LCD_D00**	MII_P0_CRS	GPIO24	LCD data bus providing a 4-, 8-, 12-, or 16-bit data path Character display mode (IN/OUT) Read and write the command and data registers Raster display mode (OUT) Constant-flow (~70 Hz) pixel data Micro-display mode (IN/OUT) Read and write the command and data registers As shown in section 5.2 "Recommended Operating Conditions" on page 90, the TNETV1056 input cells should not be driven above 3.6 V. Transceivers are required when reading from displays driving 5-V TTL signals.
AB14		**LCD_D01**	MII_P0_TX_D0	GPIO25	
AA14		**LCD_D02**	MII_P0_TX_D1	GPIO26	
Y14		**LCD_D03**	MII_P0_TX_D2	GPIO27	
AB15		**LCD_D04**	MII_P0_TX_D3	GPIO28	
AA15		**LCD_D05**	MII_P0_TX_ENBL	GPIO29	
Y15		**LCD_D06**	MII_P0_TX_CLK	GPIO30	
AB16		**LCD_D07**	MII_P0_LINK	GPIO31	
AA16		**LCD_D08**	MII_P0_COL	GPIO32	
Y16		**LCD_D09**	MII_P0_RX_ERR	GPIO33	
AB17		**LCD_D10**	MII_P0_RX_CLK	GPIO34	
AA17		**LCD_D11**	MII_P0_RX_DV	GPIO35	
Y17		**LCD_D12**	MII_P0_RX_D0	GPIO36	
W17		**LCD_D13**	MII_P0_RX_D1	GPIO37	
AB18		**LCD_D14**	MII_P0_RX_D2	GPIO38	
AA18		**LCD_D15**	MII_P0_RX_D3	GPIO39	
End of Table 3-14					

3.3.7 Sequencer Serial Port (SSP)

Within the SSP there are two state machines (serial port 0 and serial port 1). Each of these state machines provides input and output control of the standard set of serial signals (enable, clock, and data). The five TNETV1056 I/O signals (SSP[4:0]) can be multiplexed to any one of these six serial port signals. In addition, these I/O signals can be controlled as GPIOs.

Table 3-15 SSP I/Os

Terminal No.	Type	1st	2nd	3rd	Description
D3	I/O	**SSP0**			Each of these I/O signals can be multiplexed to any one of the following serial port functions: • Serial port 0 enable • Serial port 0 clock • Serial port 0 data • Serial port 1 enable • Serial port 1 clock • Serial port 1 data • GPIO input • GPIO output The input or output control, as well as the polarity of the port functions, is determined by the program in the port state machine.
D1		**SSP1**			
D2		**SSP2**			
E4		**SSP3**			
V2		GPIO05		**SSP4**	
End of Table 3-15					

3.3.8 Keypad Interface

The keypad I/O may be configured as an 8 × 8 row and column matrix, accommodating 64 keys. Activation of any key produces a debounced MIPS interrupt. The MIPS can determine which key (or keys) activated the interrupt through write sequences of the column lines.

Table 3-16 Keypad I/Os

Terminal No.	Type	1st	2nd	3rd	Description
AB7	O	**KEYPAD00**		GPIO08	Keypad column lines that should be configured as outputs. The internal pulldowns provide proper bias (OUT).
AA7		**KEYPAD01**		GPIO09	
AB8		**KEYPAD02**		GPIO10	
AA8		**KEYPAD03**		GPIO11	
Y8		**KEYPAD04**		GPIO12	
AB9		**KEYPAD05**		GPIO13	
AA9		**KEYPAD06**		GPIO14	
Y9		**KEYPAD07**		GPIO15	
AB10	I	**KEYPAD08**		GPIO16	Keypad row lines that should be configured as inputs. The internal pullups provide proper bias (IN).
AA10		**KEYPAD09**		GPIO17	
Y10		**KEYPAD10**		GPIO18	
AB11		**KEYPAD11**		GPIO19	
AA11		**KEYPAD12**		GPIO20	
W11		**KEYPAD13**		GPIO21	
Y11		**KEYPAD14**		GPIO22	
AB12		**KEYPAD15**		GPIO23	
End of Table 3-16					

3.3.9 VLYNQ Serial Communication Port

One VLYNQ serial communication interface is provided on the TNETV1056, supporting host-to-peripheral or peer-to-peer communication modes. The five-terminal version (VLYNQ5) provides a two-bit transmit and receive serial path, with clock rates up to 62.5 MHz, and can be configured to attach to either a three-terminal or five-terminal external VLYNQ-compatible device.

3.3.9.1 Five-Terminal VLYNQ Port

Table 3-17 VLYNQ5 I/Os

Terminal No.	Type	1st	2nd	3rd	Description
K3	I/O	**VLYNQ5_CLK**			VLYNQ5 serial clock (IN and OUT). This clock signal provides synchronization to VLYNQ5_RX_D0, VLYNQ5_RX_D1, VLYNQ5_TX_D0, and VLYNQ5_TX_D1. This signal can be programmed as either an internal or external source. If not used, hold high with the internal pullup.
K2	I	**VLYNQ5_RX_D0**			VLYNQ5 serial receive data. This data is coded 8-bit/10-bit data that is received on this two-bit bus as TNETV1056 read data (and requests) or as write data issued from the external VLYNQ device. If not used, hold low with an external 47-kΩ pulldown resistor.
K1		**VLYNQ5_RX_D1**			
L2	I/O	**VLYNQ5_TX_D0**			VLYNQ5 serial transmit data (OUT). This data is coded 8-bit/10-bit data that is presented on this 2-bit bus as TNETV1056 requests and TNETV1056 write data and read data in response to a request from the external VLYNQ device. VLYNQ reset configuration (IN). Two-thousand clock cycles after the VLYNQ5 subsystem is released from reset, the state of this signal determines the VLYNQ bus width. For attachment to an external VLYNQ three-terminal device, both bits must be held low with an external pulldown. For attachment to an external VLYNQ five-terminal device, D1 is held low with an external pulldown, while D0 must be held high with an external pullup. If not used, hold low with an external 47-kΩ pulldown resistor.
L1		**VLYNQ5_TX_D1**			
End of Table 3-17					

3.3.10 Universal Asynchronous Receiver/Transmitter (UART)

The UART is compliant and compatible with many standard UART implementations. Due to the 3.3-V limits of the TNETV1056 I/O, an external 5-V compliant transceiver is required for those applications requiring a 5-V driver.

Table 3-18 UART I/Os

Terminal No.	Type	1st	2nd	3rd	Description
B3	I	**UART_CTS**			Clear to send control
A3	O	**UART_RTS**			Request to send control
B4	I	**UART_RX**			Receiver data
C4	O	**UART_TX**			Transmitter data
End of Table 3-18					

3.3.11 General-Purpose I/Os (GPIOs)

The TNETV1056 provides 52 GPIOs. Of the 52 GPIOs, only 8 are dedicated for primary use. All 52 GPIOs have the following register-programmable capabilities:

- Individual enable control
- Individual input or output designation

3.3.11.1 Primary GPIOs

Table 3-19 Primary GPIOs

Terminal No.	Type	1st	2nd	3rd	Description
R3	I/O	**GPIO00**		EXT_INT1	GPIOs designated as outputs send information out of the TNETV1056 from a control register. GPIOs designated as inputs receive external information through a different control register.
T3		**GPIO01**		EXT_INT2	
U3		**GPIO02**		EXT_INT3	
T2		**GPIO03**		EXT_INT4	
U2		**GPIO04**			
V2		**GPIO05**		SSP4	
U1		**GPIO06**			
V1		**GPIO07**			
End of Table 3-19					

3.3.11.2 Multiplexed GPIOs

Table 3-20 Multiplexed GPIOs (Part 1 of 2)

Terminal No.	Type	1st	2nd	3rd	Description
AB7	I/O	KEYPAD00		**GPIO08**	GPIOs designated as outputs send information out of the TNETV1056 from a control register. GPIOs designated as inputs receive external information through a different control register.
AA7		KEYPAD01		**GPIO09**	
AB8		KEYPAD02		**GPIO10**	
AA8		KEYPAD03		**GPIO11**	
Y8		KEYPAD04		**GPIO12**	
AB9		KEYPAD05		**GPIO13**	
AA9		KEYPAD06		**GPIO14**	
Y9		KEYPAD07		**GPIO15**	
AB10		KEYPAD08		**GPIO16**	
AA10		KEYPAD09		**GPIO17**	
Y10		KEYPAD10		**GPIO18**	
AB11		KEYPAD11		**GPIO19**	
AA11		KEYPAD12		**GPIO20**	
W11		KEYPAD13		**GPIO21**	
Y11		KEYPAD14		**GPIO22**	
AB12		KEYPAD15		**GPIO23**	
Y13		LCD_D00	MII_P0_CRS	**GPIO24**	
AB14		LCD_D01	MII_P0_TX_D0	**GPIO25**	
AA14		LCD_D02	MII_P0_TX_D1	**GPIO26**	
Y14		LCD_D03	MII_P0_TX_D2	**GPIO27**	
AB15		LCD_D04	MII_P0_TX_D3	**GPIO28**	
AA15		LCD_D05	MII_P0_TX_ENBL	**GPIO29**	
Y15		LCD_D06	MII_P0_TX_CLK	**GPIO30**	
AB16		LCD_D07	MII_P0_LINK	**GPIO31**	
AA16		LCD_D08	MII_P0_COL	**GPIO32**	
Y16		LCD_D09	MII_P0_RX_ERR	**GPIO33**	
AB17		LCD_D10	MII_P0_RX_CLK	**GPIO34**	
AA17		LCD_D11	MII_P0_RX_DV	**GPIO35**	
Y17		LCD_D12	MII_P0_RX_D0	**GPIO36**	
W17		LCD_D13	MII_P0_RX_D1	**GPIO37**	
AB18		LCD_D14	MII_P0_RX_D2	**GPIO38**	
AA18		LCD_D15	MII_P0_RX_D3	**GPIO39**	

Table 3-20 Multiplexed GPIOs (Part 2 of 2)

Terminal No.	Type	1st	2nd	3rd	Description
M19	I/O	TELE_DCLK		**GPIO40**	GPIOs designated as outputs send information out of the TNETV1056 from a control register. GPIOs designated as inputs receive external information through a different control register.
N20		TELE_DI		**GPIO41**	
M20		TELE_DO		**GPIO42**	
L19		TELE_CLK_I		**GPIO43**	
M21		TELE_RINGIN1		**GPIO44**	
M22		TELE_RINGIN2		**GPIO45**	
L21		TELE_RINGIN3		**GPIO46**	
L22		TELE_RINGIN4		**GPIO47**	
L20		TELE_FS		**GPIO48**	
K20		$\overline{\text{TELE\_CS}}$		**GPIO49**	
K21		TELE_INT		**GPIO50**	
K22		$\overline{\text{TELE\_RESET}}$		**GPIO51**	
End of Table 3-20					

3.3.11.3 Additional GPIOs

Certain TNETV1056 subsystems provide additional GPIO terminal capabilities as shown in Table 3-21. The control for these GPIO terminals is retained in the defined subsystem rather than the GPIO subsystem.

Table 3-21 Additional GPIOs (Part 1 of 2)

Terminal No.	Type	1st	2nd	3rd	Description
D3	I/O	**SSP0**			These SSP subsystem I/O signals can be configured as GPIOs (see section 3.3.7 "Sequencer Serial Port (SSP)" on page 44).
D1		**SSP1**			
D2		**SSP2**			
E4		**SSP3**			
V2		GPIO05		**SSP4**	
M3	I/O	**McBSP_CLK_RX**			These McBSP subsystem I/O signals can be configured as GPIOs (see section 3.3.4 "Multichannel Buffered Serial Port (McBSP) Interface" on page 41).
N3	I	**McBSP_D_RX**			
P2	I/O	**McBSP_FS_RX**			
N2	I/O	**McBSP_CLK_TX**			
P1	O	**McBSP_D_TX**			
P3	I/O	**McBSP_FS_TX**			

Table 3-21 Additional GPIOs (Part 2 of 2)

Terminal No.	Type	1st	2nd	3rd	Description
AB7	I/O	**KEYPAD00**		GPIO08	Any keypad terminal may be used as a GPIO when not in use as a keypad. There is no need to select the GPIO function placed on the 3rd I/O multiplexer.
AA7		**KEYPAD01**		GPIO09	
AB8		**KEYPAD02**		GPIO10	
AA8		**KEYPAD03**		GPIO11	
Y8		**KEYPAD04**		GPIO12	
AB9		**KEYPAD05**		GPIO13	
AA9		**KEYPAD06**		GPIO14	
Y9		**KEYPAD07**		GPIO15	
AB10		**KEYPAD08**		GPIO16	
AA10		**KEYPAD09**		GPIO17	
Y10		**KEYPAD10**		GPIO18	
AB11		**KEYPAD11**		GPIO19	
AA11		**KEYPAD12**		GPIO20	
W11		**KEYPAD13**		GPIO21	
Y11		**KEYPAD14**		GPIO22	
AB12		**KEYPAD15**		GPIO23	
End of Table 3-21					

3.3.12 MIPS Interrupt

Table 3-22 MIPS Interrupt I/Os

Terminal No.	Type	1st	2nd	3rd	Description
R3	I/O	GPIO00		**EXT_INT1**	Interrupt 1 (IN). This external interrupt enters the MIPS as INT_1.
T3	I/O	GPIO01		**EXT_INT2**	Interrupt 2 (IN). This external interrupt enters the MIPS as INT_2.
U3	I/O	GPIO02		**EXT_INT3**	Interrupt 3 (IN). This external interrupt enters the MIPS as INT_3.
T2	I/O	GPIO03		**EXT_INT4**	Interrupt 4 (IN). This external interrupt enters the MIPS as INT_4.
K21	I/O	**TELE_INT**		GPIO50	Telephony interface subsystem interrupt (IN). This external interrupt enters the MIPS as INT_23 and the DSP as DSP_INT_12. This is the only externally-sourced DSP interrupt signal.
End of Table 3-22					

3.3.13 JTAG

3.3.13.1 MIPS and ASIC

This enhanced JTAG (EJTAG) compliant port provides MIPS emulation control, MIPS boundary-scan control, and ASIC boundary-scan control. The ASIC boundary scan encompasses all TNETV1056 logic including the MIPS and DSP, but excludes the analog I/O signals found in the internal PHY devices and internal voice codec device. Except for the internal pulldown configuration on several of the I/Os, this JTAG implementation is IEEE Std 1149.1 compliant. To access the device JTAG model for boundary scan testing, set $\overline{\text{EJTAG\_TRST1}}$ high and set $\overline{\text{EJTAG\_TRST0}}$ low. To access the MIPS EJTAG model for emulation, set $\overline{\text{EJTAG\_TRST1}}$ low and set $\overline{\text{EJTAG\_TRST0}}$ high. The DSP JTAG module is enabled by setting $\overline{\text{JTAG\_TRST}}$ high.

Table 3-23 MIPS JTAG I/Os

Terminal No.	Type	1st	2nd	3rd	Description
E3	I	**EJTAG_DINT**			MIPS and ASIC JTAG exception request. If not used, hold high (with internal pullup).
E2	I	**$\overline{\text{EJTAG\_SYSRST}}$**			Similar function as $\overline{\text{RESET\_I}}$. If not used, hold high (with internal pullup). Do not use this signal.
F3	I	**$\overline{\text{EJTAG\_TRST0}}$**			MIPS JTAG test reset. If not used, hold low (with internal pulldown). An external pullup should not be used.
E1	I	**$\overline{\text{EJTAG\_TRST1}}$**			ASIC JTAG test reset. If not used, hold low (with internal pulldown). An external pullup should not be used.
F2	I	**EJTAG_TCK**			MIPS and ASIC JTAG test clock. If not used, hold high (with internal pullup).
G3	I	**EJTAG_TDI**			MIPS and ASIC JTAG test data input. If not used, hold high (with internal pullup).
F1	O	**EJTAG_TDO**			MIPS and ASIC JTAG test data output
G2	I	**EJTAG_TMS**			MIPS and ASIC JTAG test mode select. If not used, hold high (with internal pullup).
End of Table 3-23					

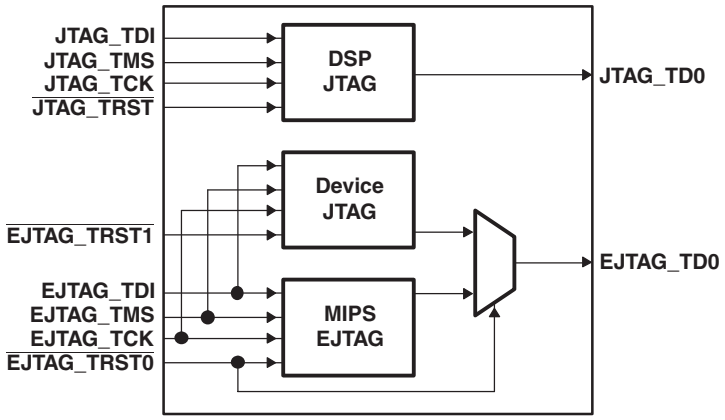
3.3.13.2 DSP

This JTAG-compliant port provides DSP emulation control and DSP boundary-scan control. Besides the internal pulldown configuration on several of the I/Os, this JTAG implementation is IEEE Std 1149.1 compliant.

Table 3-24 DSP JTAG I/Os

Terminal No.	Type	1st	2nd	3rd	Description
H3	I/O	**JTAG_EMU0**			DSP special-emulation control modes. If not used, hold high (with internal pullup).
G1		**JTAG_EMU1**			
H2	I	**$\overline{\text{JTAG\_TRST}}$**			DSP JTAG test reset. If not used, hold low (with internal pulldown). An external pullup should not be used.
J3	I	**JTAG_TCK**			DSP JTAG test clock. If not used, hold high (with internal pullup).
H1	I	**JTAG_TDI**			DSP JTAG test data input. If not used, hold high (with internal pullup).
J2	O	**JTAG_TDO**			DSP JTAG test data output
J1	I	**JTAG_TMS**			DSP JTAG test mode select. If not used, hold high (with internal pullup).
End of Table 3-24					

Figure 3-4 JTAG I/Os



3.3.14 System Clock and Reset

Table 3-25 Clock and Reset I/Os

Terminal No.	Type	1st	2nd	3rd	Description
P22	I/O	**REF_CLK_I**			Differential crystal pair for the entire TNETV1056 (except the voice codec) (see Figure 3-5 for the TNETV1056 clock structure)
N22	O	**REF_CLK_O**			The target input frequency is 25 MHz.
P21	I	**ALT_CLK_I**			Alternate non-crystal clock input. This clock can be programmed to replace the REF_CLK in any TNETV1056 subsystem (see Figure 3-5 for the TNETV1056 clock structure). The target input frequency is 25 MHz.
R1	I/O	**AIC_CLK_I**			Differential crystal pair for the internal voice codec clock (see Figure 3-5 for the TNETV1056 clock structure)
T1	O	**AIC_CLK_O**			The recommended frequency is 8.1920 MHz.
C1	I	**$\overline{\text{RESET\_I}}$**			Reset input for the TNETV1056 is provided by the external power-on-reset supervisor.
C2	O	**$\overline{\text{RESET\_O}}$**			Reset output from the TNETV1056 is register controlled (on/off), as well as activated, by $\overline{\text{RESET\_I}}$.
E2	I	**$\overline{\text{EJTAG\_SYSRST}}$**			Similar function as $\overline{\text{RESET\_I}}$. If not used, hold high (with internal pullup). Do not use this signal.
K22	I/O	**$\overline{\text{TELE\_RESET}}$**		GPIO51	Telephony interface subsystem reset (OUT). This reset is activated by $\overline{\text{RESET\_I}}$ and register control in the DSP subsystem.
End of Table 3-25					

3.3.15 Power

3.3.15.1 I/O

Table 3-26 I/O Power

Terminal No.	Type	1st	2nd	3rd	Description
D7	P	**VDDS**			3.3-V power supply for the I/O ring
D8		**VDDS**			
D9		**VDDS**			
D10		**VDDS**			
D13		**VDDS**			
D14		**VDDS**			
D15		**VDDS**			
D16		**VDDS**			
G4		**VDDS**			
G19		**VDDS**			
H4		**VDDS**			
H19		**VDDS**			
J4		**VDDS**			
J19		**VDDS**			
K4		**VDDS**			
K19		**VDDS**			
N4		**VDDS**			
P4		**VDDS**			
W9		**VDDS**			
W10		**VDDS**			
W13		**VDDS**			
W14		**VDDS**			
W15		**VDDS**			
W16		**VDDS**			
End of Table 3-26					

3.3.15.2 Core

Table 3-27 Core Power

Terminal No.	Type	1st	2nd	3rd	Description
J10	P	**VDD**			1.5-V power supply for the logic core If the internal voltage regulator is used, this power is provided by the external npn pass transistors.
J11		**VDD**			
J12		**VDD**			
J13		**VDD**			
K9		**VDD**			
K14		**VDD**			
L9		**VDD**			
L14		**VDD**			
M9		**VDD**			
M14		**VDD**			
N9		**VDD**			
N14		**VDD**			
P10		**VDD**			
P11		**VDD**			
P12		**VDD**			
P13		**VDD**			
AB6		**VDD**			
End of Table 3-27					

3.3.15.3 Analog

Table 3-28 Analog Power

Terminal No.	Type	1st	2nd	3rd	Description
N19	P	**VDD_PLL**			1.5-V isolated supply power for the internal analog PLL devices
R4	P	**VDDA_AIC**			3.3-V isolated analog logic supply power for the internal voice codec (see VSS_AIC)
T4		**VDDA_AIC**			
W7		**VDDA_AIC**			
W8		**VDDA_AIC**			
U21	P	**VDDA_PHY0_1**			3.3-V isolated analog supply power for internal Ethernet PHY port 0 (TX)
U20	P	**VDDA_PHY0_2**			3.3-V isolated analog supply power for internal Ethernet PHY port 0 (RX and ADC)
Y20	P	**VDDA_PHY0_34**			3.3-V isolated analog supply power for internal Ethernet PHY port 0 (all other internal circuits)
U22	P	**VDDA_PHY1_1**			3.3-V isolated analog supply power for unused internal Ethernet PHY port 1 (TX). Must be connected.
U19	P	**VDDA_PHY1_2**			3.3-V isolated analog supply power for unused internal Ethernet PHY port 1 (RX and ADC). Must be connected.
P20	P	**VDDA_PHY1_34**			3.3-V isolated analog supply power for unused internal Ethernet PHY port 1 (all other internal circuits). Must be connected.
End of Table 3-28					

3.3.16 Ground

3.3.16.1 Digital

Table 3-29 Digital Ground

Terminal No.	Type	1st	2nd	3rd	Description
A1	G	**VSS**			Ground
A2		**VSS**			
A21		**VSS**			
A22		**VSS**			
B1		**VSS**			
B2		**VSS**			
B21		**VSS**			
B22		**VSS**			
C3		**VSS**			
C20		**VSS**			
D4		**VSS**			
D19		**VSS**			
J9		**VSS**			
J14		**VSS**			
K10		**VSS**			
K11		**VSS**			
K12		**VSS**			
K13		**VSS**			
L10		**VSS**			
L11		**VSS**			
L12		**VSS**			
L13		**VSS**			
M10		**VSS**			
M11		**VSS**			
M12		**VSS**			
M13		**VSS**			
N10		**VSS**			
N11		**VSS**			
N12		**VSS**			
N13		**VSS**			
End of Table 3-29					

3.3.16.2 Analog

Table 3-30 Analog Ground

Terminal No.	Type	1st	2nd	3rd	Description
W4	G	**VSS_AIC**			Isolated analog ground for the internal voice codec (see VDDA_AIC)
Y3		**VSS_AIC**			
AA1		**VSS_AIC**			
AA2		**VSS_AIC**			
AB1		**VSS_AIC**			
AB2		**VSS_AIC**			
V21	G	**VSS_PHY0_1**			Isolated analog ground for internal Ethernet PHY port 0 (TX)
W21		**VSS_PHY0_1**			
V20	G	**VSS_PHY0_2**			Isolated analog ground for internal Ethernet PHY port 0 (RX and ADC)
W20	G	**VSS_PHY0_34**			Isolated analog ground for internal Ethernet PHY port 0 (all other internal circuits)
V19	G	**VSS_PHY0_ESD**			ESD-specific ground for internal Ethernet PHY port 0
R21	G	**VSS_PHY1_1**			Isolated analog ground for unused internal Ethernet PHY port 1 (TX). Must be connected.
T21		**VSS_PHY1_1**			
T20	G	**VSS_PHY1_2**			Isolated analog ground for unused internal Ethernet PHY port 1 (RX and ADC). Must be connected.
R20	G	**VSS_PHY1_34**			Isolated analog ground for unused internal Ethernet PHY port 1 (all other internal circuits). Must be connected.
T19	G	**VSS_PHY1_ESD**			ESD-specific ground for unused internal Ethernet PHY port 1. Must be connected.
P14	G	**VSS_PLL**			Isolated ground for the internal analog PLL devices
N21	G	**VSS_REF_CLK**			Isolated ground for the REF_CLK oscillator (see REF_CLK_I and REF_CLK_O). This V_{SS} terminal remains independent of all other V_{SS} terminals and must not be connected to the common board ground.
P9	G	**VSS_AIC_CLK**			Isolated ground for the voice codec oscillator (see AIC_CLK_I and AIC_CLK_O). This V_{SS} terminal remains independent of all other V_{SS} terminals and must not be connected to the common board ground.
End of Table 3-30					

3.3.17 Voltage Regulators

Two internal voltage regulators are required to supply the power consumption needs of the TNETV1056 VDD (1.5 V) core voltage. The maximum supply current capacity of these two voltage regulators is 1.33 A. The necessary 1.2-V bandgap reference is created internally (with an additional small voltage regulator) through the VDDS (3.3 V) power rail. As shown in Table 3-31and Figure 4-7, two external npn pass transistors are required to regulate voltage into the TNETV1056. In addition, one 10-µF tantalum capacitor is necessary in the external-regulator design. TI recommends a 2.0-W supply be used for the 3.3-V (V_{DDS}) power rail and that the internal voltage regulator be used to generate the 1.5-V (V_{DD}) core voltage. This provides margin for the TNETV1056 to power up.

Table 3-31 Voltage Regulator I/Os

Terminal No.	Type	1st	2nd	3rd	Description
R2	O	**VR_BASE2**			Voltage regulator 2 drive to the base of external npn pass transistor two
Y22	O	**VR_BASE3**			Voltage regulator 3 drive to the base of external npn pass transistor three
AA6	I	**$\overline{\text{VR\_ENBL}}$**			Voltage regulator enable. When high (3.3 V), the internal regulators are in power-down mode. When low (0 V), the regulators are functional, and power for VDD (1.5 V) can be supplied from the external npn pass transistors.
End of Table 3-31					

3.3.18 Test

Table 3-32 Test I/Os

Terminal No.	Type	1st	2nd	3rd	Description
F4	I	**TEST**			For normal operation, must be held low (with internal pulldown).
Y21	I	**PHY_TEST**			For normal operation, must be held low with external pulldown.
Y12	I/O	LCD_PIXEL_STRB	**DSP_FUNCTEST0**		For test purposes only. Do not select multiplexer for use.
AB13	I/O	LCD_E1	**DSP_FUNCTEST1**		For test purposes only. Do not select multiplexer for use.
End of Table 3-32					

3.3.19 No Connection

Table 3-33 No Connection Terminals

Terminal No.	Type	Description
L3, L4, M1, M2, M4, N1, P19, R19, R22, T22, AA21, AA22, AB22	N/C	No connection. Do not bias. These terminals may be connected internally. Do not use as a routing point.
End of Table 3-33		

3.4 Boot Configuration

Certain TNETV1056 I/O terminals provide a boot-configuration option. These special I/O terminals read the state of the incoming signal at $\overline{\text{RESET\_I}}$ deactivation and store the received value for the uses shown in Table 3-34. Many of the stored values can be viewed in the SYS_CONFIG (BOOT) register. External pullup or pulldown resistors should be placed on these boot configuration I/O terminals to obtain the desired results.

Table 3-34 Boot Configuration I/Os

External Terminal	Register		Default Bit Code	Description
	Name	Bit		
EM_A[23:22]	FLASH_WIDTH	8:7	01	Flash width. Defines the flash ($\overline{\text{EM\_CS0}}$) data bus width. 11 = 32-bit flash 10 = 32-bit flash 01 = 16-bit flash 00 = 8-bit flash The width of the flash data bus may be adjusted through program control using the EMIF (ASYNCHRONOUS_CONFIG_BANK_1) register.
EM_A[21]	ENDIAN_MODE	6	N/A	Endian mode. Defines the endian operating mode for the TNETV1056. 1 = Big endian 0 = Little endian A default is not available. This bit must be programmed externally, even when DEFAULT = 1.
EM_A[20:18]	BOOT_SELECT	2:0	001	Boot memory location select. The MIPS processor always starts the TNETV1056 boot from the internal 4K-byte ROM. Within this ROM, the MIPS code interrogates these bits and determines where the rest of the boot code resides. 111 = Boot from VLYNQ5 port 110 = Boot from serial EEPROM through the SSP 101 = Boot from $\overline{\text{EM\_CS5}}$ (asynchronous memory) 100 = Boot from $\overline{\text{EM\_CS4}}$ (asynchronous memory) 011 = Boot from $\overline{\text{EM\_CS3}}$ (asynchronous memory) 010 = Boot from $\overline{\text{EM\_CS1}}$ and $\overline{\text{EM\_CS2}}$ (SDRAM) 001 = Boot from $\overline{\text{EM\_CS0}}$ (flash) 000 = Boot from internal 4K-Byte ROM only The boot location value may be adjusted through program control using the BOOT_OVERRIDE bits in the SYS_CONFIG (BOOT) register.
EM_A[17]	PLL_MODE	5	0	PLL mode. As shown in Figure 3-5, several TNETV1056 PLL generators can be bypassed. 1 = Bypass the PLL, for test-mode use only 0 = Use the standard PLL configuration
EM_A[16]	WD_MODE (inverted)	4	0	System watchdog timer disable mode. This terminal may be used to permanently disable the system watchdog timer. The WD_MODE register bit contents are inverted from the following definition. 1 = System watchdog timer is always disabled. 0 = System watchdog timer may be enabled (see EM_A15).
EM_A[15]	WD_WR_MODE	3	0	System watchdog timer write protect mode. This terminal may be used to generate a write protect feature, permanently preventing any changes to the TIMER_ENABLE bit in the SYS_TIMER_WD (ENABLE) register. 1 = The system watchdog timer is write protected. The operational state of the timer is determined from the reset contents of the TIMER_ENABLE bit in the SYS_TIMER_WD (ENABLE) register. 0 = The system watchdog timer may be enabled and disabled through the use of the TIMER_ENABLE bit in the SYS_TIMER_WD (ENABLE) register.

Table 3-34 Boot Configuration I/Os

External Terminal	Register		Default Bit Code	Description
	Name	Bit		
EM_A[14]	SDRAM_MODE	9	1	EMIF SDRAM clock mode. The EMIF external clock EM_CLK (SDRAM clock) may be programmed for half speed (VBUSP_CLK/2). In either mode, the SDRAM and asynchronous memory external timing follows the clock speed. Thus, the EMIF external timing runs at one-half rate when selected for half-speed mode. 1 = EMIF runs at full speed (VBUSP_CLK) 0 = EMIF runs at half speed (½ VBUSP_CLK)
EM_A[13]	SDRAM_INIT	10	0	EMIF SDRAM initialization mode. The SDRAM initialization sequence is reduced by forcing the SDRAM refresh counter to a minimum value as defined in the EMIF (SDRAM_REFRESH_CTRL) register. This minimum time value drastically reduces the long delay at the start of the SDRAM initialization. 1 = Reduced SDRAM initialization timing for test purposes 0 = Normal SDRAM initialization operation
EM_A[12:11]	VBUSP_CLOCK	15:14	01	VBUSP clock input multiplexer select. As shown in Figure 3-5, the input clock source for the VBUSP_CLK is determined by the state of these I/O terminals: 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Voice codec clock I/O (AIC_CLK_I and AIC_CLK_O) This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register. Due to metastability issues, program-controlled adjustment is not recommended.
EM_A[10:9]	NC_CLOCK	17:16	01	No connect input multiplexer select. These I/Os should be programmed to the same stae as the MIPS_CLOCK bits EM_A[3:2]. This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register. Due to metastability issues, program-controlled adjustment is not recommended.
EM_A[8:7]	PHY_CLOCK	19:18	01	Ethernet PHY clock input multiplexer select (see Figure 3-5). The input clock source for the Ethernet PHY_CLK is determined by the state of these I/O terminals: 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Voice codec clock I/O (AIC_CLK_I and AIC_CLK_O) This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register. Due to metastability issues, program-controlled adjustment is not recommended.
EM_A[6:5]	DSP_CLOCK	21:20	01	DSP clock input multiplexer select (see Figure 3-5). The input clock source for the DSP_CLK is determined by the state of these I/O terminals: 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Voice codec clock I/O (AIC_CLK_I and AIC_CLK_O) This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register. Due to metastability issues, program-controlled adjustment is not recommended.
EM_A[4]	NC_MODE	22	1	No connect mode. This I/O should be programmed to the default value. This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register.

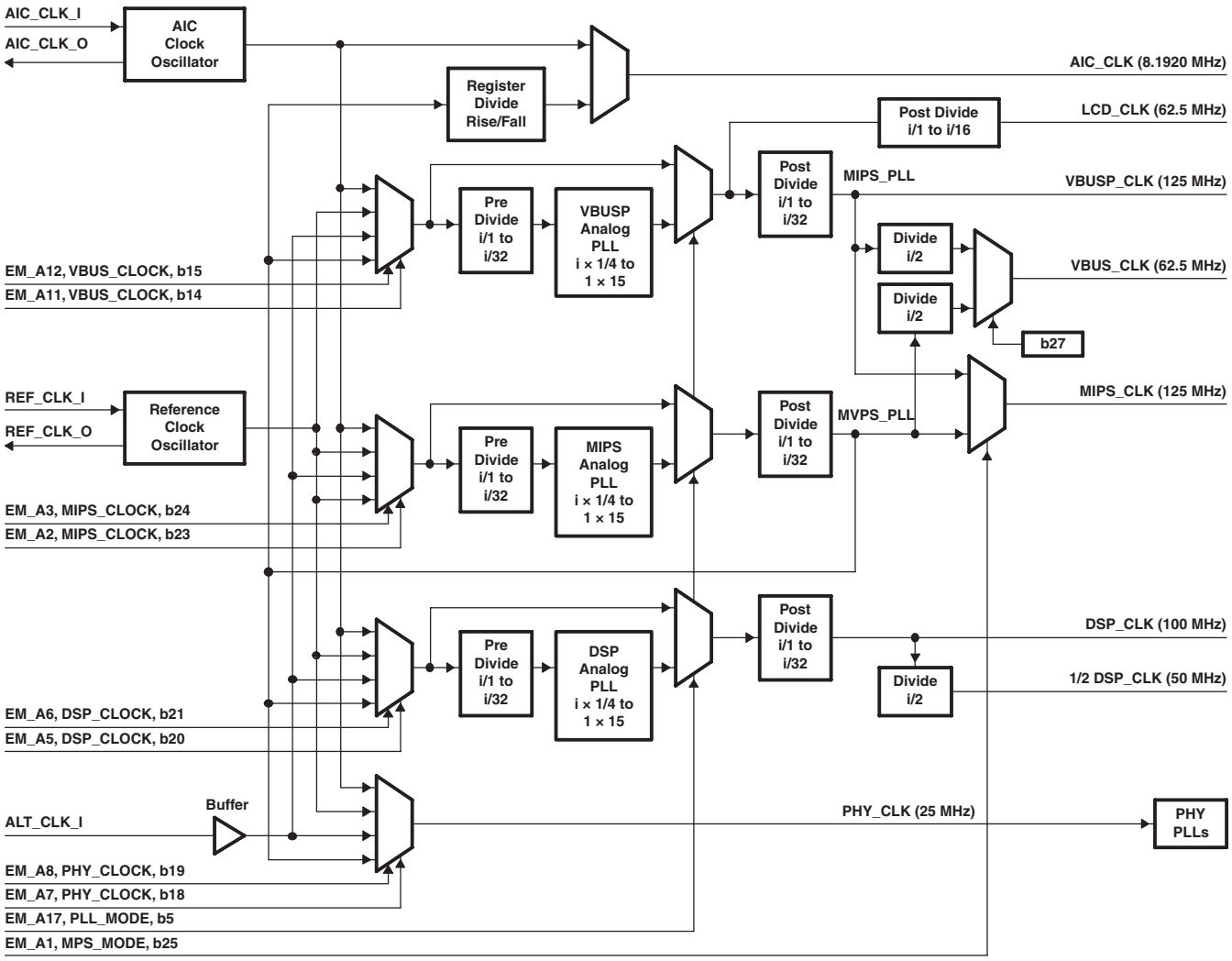
Table 3-34 Boot Configuration I/Os

External Terminal	Register		Default Bit Code	Description
	Name	Bit		
EM_A[3:2]	MIPS_CLOCK	24:23	01	MIPS clock input multiplexer select (see Figure 3-5). The input clock source for the MIPS_CLK is determined by the state of these I/O terminals: 11 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Voice codec clock I/O (AIC_CLK_I and AIC_CLK_O) This boot configuration value may be adjusted through program control using the SYS_CONFIG (BOOT) register. Due to metastability issues, program-controlled adjustment is not recommended.
EM_A[1]	MIPS_MODE	25	1	MIPS clock mode (see Figure 3-5). The clock source for the MIPS_CLK may be synchronous utilizing the VBUSP_CLK or asynchronous derived from the MIPS PLL. 1 = MIPS_CLK is asynchronous. 0 = MIPS_CLK is synchronous.
EM_A[0]	DEFAULT	26	N/A	Default control. Defines the $\overline{\text{RESET\_I}}$ contents of the SYS_CONFIG (BOOT) register. 1 = Boot configuration is defined by the Default field in this table, initialization state of EM_A[23:01] is ignored. 0 = Initialization state of EM_A[23:01] determines the boot configuration.
VLYNQ5_TX_D0 VLYNQ5_TX_D1	N/A	N/A	N/A	VLYNQ 5-terminal configuration. After a VLYNQ 5-terminal subsystem reset event, the state of this signal determines the VLYNQ bus width. • For attachment to an external VLYNQ 3-terminal device, both bits must be held low with an external pulldown. • For attachment to an external VLYNQ 5-terminal device, VLYNQ5_TX_D1 is held low with an external pulldown while VLYNQ5_TX_D0 must be held high with an external pullup.

3.4.1 Clock Distribution

Figure 3-5 shows the TNETV1056 clock distribution network. As shown inTable 3-34, the multiplexed selection network is defined at $\overline{\text{RESET\_I}}$ deactivation through the use of the special boot configuration I/O terminals.

Figure 3-5 TNETV1056 Clock Distribution



NOTE: All bits (b#) are contained in SYS_CONFIG (BOOT).

3.4.2 SYS_CONFIG (BOOT)

Bits [31:08] of the 32-bit VBUSP address bus define the block location of the system configuration controller (SYS_CONFIG) starting at 0x0861:1A00 and ending at 0x0861:1AFF. Address bits [7:0] are used to define each 32-bit-wide address location within the SYS_CONFIG block. The SYS_CONFIG block only uses address bits [3:0], thus, register addressing greater than 0x0861:1A0F allows aliased writes and reads of SYS_CONFIG registers in the range 0x0861:1A00 to 0x0861:1A0F. The bit map is shown in Table 3-35, with bit descriptions shown in Table 3-36.

Table 3-35 SYS_CONFIG (BOOT) Register

Address: 0x0861:1A00								
Bit	31	30	29	28	27	26	25	24
Name	Reserved				VBUS_MODE	DEFAULT (rd-only)	MIPS_MODE (rd-only)	MIPS_CLOCK
Reset 0 **Reset 1**	0 0	0 0	0 0	0 0	0 0	EM_A0 EM_A0	EM_A1 1	EM_A3 0
Bit	23	22	21	20	19	18	17	16
Name	MIPS_CLOCK	NC_MODE	DSP_CLOCK		PHY_CLOCK		NC_CLOCK	
Reset 0 **Reset 1**	EM_A2 1	EM_A4 1	EM_A6 0	EM_A5 1	EM_A8 0	EM_A7 1	EM_A10 0	EM_A9 1
Bit	15	14	13	12	11	10	9	8
Name	VBUSP_CLOCK		BOOT_OVERRIDE			SDRAM_INIT (rd-only)	SDRAM_MODE (rd-only)	FLASH_WIDTH (rd-only)
Reset 0 **Reset 1**	EM_A12 0	EM_A11 1	0 0	0 0	0 0	EM_A13 0	EM_A14 1	EM_A23 0
Bit	7	6	5	4	3	2	1	0
Name	FLASH_WIDTH (rd-only)	ENDIAN_MODE (rd-only)	PLL_MODE (rd-only)	WD_MODE (rd-only)	WD_WR_ MODE (rd-only)	BOOT_SELECT (rd-only)		
Reset 0 **Reset 1**	EM_A22 1	EM_A21 EM_A21	EM_A17 0	EM_A16 1	EM_A15 0	EM_A20 0	EM_A19 0	EM_A18 1

Table 3-36 SYS_CONFIG (BOOT) Register Bits (Part 1 of 3)

Bit	Name	Description
31:28	Reserved	Always returns zero when read
27	VBUS_MODE	VBUS clock mode. The state of this bit determines the VBUS_CLK source (see Figure 3-5). 1 = VBUS_CLK = ½(MIPS PLL output after the post divider) 0 = VBUS_CLK = ½(VBUSP_CLK) Because this bit is adjusted through program control, all VBUS_CLK receiver logic must have clocks powered off through the SYS_CLK (PWR_DWN) register. In addition, the same VBUS_CLK receiver logic should be held in reset through the SYS_RESET (PERIPH_CTRL) register. Failure to follow these precautions can introduce metastability, causing undesirable system problems.
26	DEFAULT	Default control (read only). The state of this bit is always determined by EM_A0 after a $\overline{\text{RESET\_I}}$ event (see Table 3-34). The contents of the rest of the bits in this register depend on the state of this bit after an $\overline{\text{RESET\_I}}$ event: 1 = Reset 1 event = Content of the bits in this register are fixed by the hardware. 0 = Reset 0 event = Content of the bits in this register are dependent on the state of EM_A[23:01].
25	MIPS_MODE	MIPS clock mode (read only). The state of this bit is determined by EM_A1 after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3-34). 1 = MIPS_CLK is asynchronous. 0 = MIPS_CLK is synchronous.

Table 3-36 SYS_CONFIG (BOOT) Register Bits (Part 2 of 3)

Bit	Name	Description
24:23	MIPS_CLOCK	MIPS clock input multiplexer select. The state of these bits is determined by EM_A[3:2] after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3-34). 11 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Voice codec clock I/O (AIC_CLK_I and AIC_CLK_O) In addition, these bits may be changed through program control. This program control change is not glitch free and can introduce metastability, causing undesirable system problems. To avoid the introduction of metastability, do not change these bits through program control.
22	NC_MODE	No connect mode. The state of this bit is determined by EM_A4 after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3-34). In addition, this bit may be changed through program control.
21:20	DSP_CLOCK	DSP clock input multiplexer select. The state of these bits is determined by EM_A[6:5] after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3-34). 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Voice codec clock I/O (AIC_CLK_I and AIC_CLK_O) In addition, these bits may be changed through program control. This program control change is not glitch free and can introduce metastability, causing undesirable system problems. To avoid the introduction of metastability, do not change these bits through program control.
19:18	PHY_CLOCK	Ethernet clock input multiplexer select. The state of these bits is determined by EM_A[8:7] after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3-34). 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Voice codec clock I/O (AIC_CLK_I and AIC_CLK_O) In addition, these bits may be changed through program control. This program control change is not glitch free and can introduce metastability, causing undesirable system problems. To avoid the introduction of metastability, do not change these bits through program control.
17:16	NC_CLOCK	No connect input multiplexer select. The state of these bits is determined by EM_A[10:09] after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3-34). In addition, these bits may be changed through program control. This program control change is not glitch free and can introduce metastability, causing undesirable system problems. To avoid the introduction of metastability, do not change these bits through program control.
15:14	VBUSP_CLOCK	VBUSP clock input multiplexer select. The state of these bits is determined by EM_A[12:11] after a $\overline{\text{RESET\_I}}$ event when DEFAULT = 0b (see Table 3-34). 11 = Internal MIPS PLL clock output 10 = Alternate clock I/O (ALT_CLK_I) 01 = Reference clock I/O (REF_CLK_I and REF_CLK_O) 00 = Voice codec clock I/O (AIC_CLK_I and AIC_CLK_O) In addition, these bits may be changed through program control. This program control change is not glitch free and can introduce metastability, causing undesirable system problems. To avoid the introduction of metastability, do not change these bits through program control.

Table 3-36 SYS_CONFIG (BOOT) Register Bits (Part 3 of 3)

Bit	Name	Description
13:11	BOOT_OVERRIDE	Boot select overide. These bits may be adjusted through program control in order to override the BOOT_SELECT configuration bits contained in this same register. Reset events not employing the RESET_I input terminal are able to boot from a location other than the one defined by BOOT_SELECT. 111 = Boot from VLYNQ5 port 110 = Boot from serial EEPROM through the sequencer serial port 101 = Boot from EM_CS5 (asynchronous memory) 100 = Boot from EM_CS4 (asynchronous memory) 011 = Boot from EM_CS3 (asynchronous memory) 010 = Boot from EM_CS1 and EM_CS2 (SDRAM) 001 = Boot from EM_CS0 (flash) 000 = Ignore this BOOT_OVERIDE, the BOOT_SELECT bits in this same register define the boot location.
10	SDRAM_INIT	EMIF SDRAM initialization mode (read only). The state of this bit is determined by EM_A13 after a RESET_I event when DEFAULT = 0b (see Table 3-34). 1 = Reduced SDRAM initialization timing for test purposes 0 = Normal SDRAM initialization operation
9	SDRAM_MODE	EMIF SDRAM clock mode (read only). The state of this bit is determined by EM_A14 after a RESET_I event when DEFAULT = 0b (see Table 3-34). 1 = EMIF runs at full speed (VBUSP_CLK). 0 = EMIF runs at one-half speed (½ VBUSP_CLK).
8:7	FLASH_WIDTH	FLASH width (read only). The state of these bits is determined by EM_A[23:22] after a RESET_I event when DEFAULT = 0b (see Table 3-34). 11 = 32-bit flash 10 = 32-bit flash 01 = 16-bit flash 00 = 8-bit flash
6	ENDIAN_MODE	Endian mode (read only). The state of this bit is determined by EM_A21 after a RESET_I event, regardless of the state of DEFAULT (see Table 3-34). 1 = Big endian 0 = Little endian
5	PLL_MODE	PLL mode (read only). The state of this bit is determined by EM_A17 after a RESET_I event whenDEFAULT = 0b (see Table 3-34). 1 = Bypass the PLL, for test-mode use only 0 = Use the standard PLL configuration
4	WD_MODE	Watchdog timer disable mode (read only). The state of this bit is determined by inverted contents of EM_A16 after a RESET_I event when DEFAULT = 0b (see Table 3-34). 1 = System watchdog timer may be enabled, see AD_WR_MODE. 0 = System watchdog timer is always disabled.
3	WD_WR_MODE	System watchdog timer write protect mode (read only). The state of this bit is determined by EM_A15 after a RESET_I event (see Table 3-34). 1 = The system watchdog timer is write protected. The operational state of the timer is determined from the reset contents of the TIMER_ENABLE bit in the SYS_TIMER_WD (ENABLE) register. 0 = The system watchdog timer may be enabled and disabled through the use of the TIMER_ENABLE bit in the SYS_TIMER_WD (ENABLE) register.
2:0	BOOT_SELECT	Boot memory location select (read only). The state of these bits is determined by EM_A[20:18] after a RESET_I event when DEFAULT = 0b (see Table 3-34). 111 = Boot from VLYNQ5 port 110 = Boot from serial EEPROM through the sequencer serial port 101 = Boot from EM_CS5 (asynchronous memory) 100 = Boot from EM_CS4 (asynchronous memory) 011 = Boot from EM_CS3 (asynchronous memory) 010 = Boot from EM_CS1 and EM_CS2 (SDRAM) 001 = Boot from EM_CS0 (flash) 000 = Boot from internal 4K-byte ROM only
End of Table 3-36		

3.5 Multiplex Configuration

The TNETV1056 contains 324 I/O terminals, many of which provide multiple I/O functional modes. The I/Os featuring multiple functional modes are shown in Table 3-3. The SYS_RESET (PIN_SEL_NO) register set may be used to individually select the desired functionality of each TNETV1056 I/O terminal. The entire register set is shown in Table 3-37.

All of the terminals with multiple I/O functional modes are set to the nonfunctional 3-state mode by power-on reset (POR). To be used, these I/O terminals must be programmed as shown in Table 3-37.

Table 3-37 SYS_RESET (PIN_SEL) Register Set

Address	BLOCK Function	Name	Description
0x0861:160C	SYS_RESET	PIN_SEL_1	I/O multiplex pin select 1
0x0861:1610	SYS_RESET	PIN_SEL_2	I/O multiplex pin select 2 (N/A, no multiplexed I/O in this set)
0x0861:1614	SYS_RESET	PIN_SEL_3	I/O multiplex pin select 3 (N/A, no multiplexed I/O in this set)
0x0861:1618	SYS_RESET	PIN_SEL_4	I/O multiplex pin select 4
0x0861:161C	SYS_RESET	PIN_SEL_5	I/O multiplex pin select 5
0x0861:1620	SYS_RESET	PIN_SEL_6	I/O multiplex pin select 6 (N/A, no multiplexed I/O in this set)
0x0861:1624	SYS_RESET	PIN_SEL_7	I/O multiplex pin select 7
0x0861:1628	SYS_RESET	PIN_SEL_8	I/O multiplex pin select 8
0x0861:162C	SYS_RESET	PIN_SEL_9	I/O multiplex pin select 9
0x0861:1630	SYS_RESET	PIN_SEL_10	I/O multiplex pin select 10
0x0861:1634	SYS_RESET	PIN_SEL_11	I/O multiplex pin select 11
0x0861:1638	SYS_RESET	PIN_SEL_12	I/O multiplex pin select 12 (N/A, no multiplexed I/O in this set)
0x0861:163C	SYS_RESET	PIN_SEL_13	I/O multiplex pin select 13
0x0861:1640	SYS_RESET	PIN_SEL_14	I/O multiplex pin select 14
0x0861:1644	SYS_RESET	PIN_SEL_15	I/O multiplex pin select 15 (N/A, no multiplexed I/O in this set)
0x0861:1648	SYS_RESET	PIN_SEL_16	I/O multiplex pin select 16 (N/A, no multiplexed I/O in this set)
0x0861:164C	SYS_RESET	PIN_SEL_17	I/O multiplex pin select 17 (N/A, no multiplexed I/O in this set)
0x0861:1650	SYS_RESET	PIN_SEL_18	I/O multiplex pin select 18 (N/A, no multiplexed I/O in this set)
0x0861:1654	SYS_RESET	PIN_SEL_19	I/O multiplex pin select 19 (N/A, no multiplexed I/O in this set)
0x0861:1658	SYS_RESET	PIN_SEL_20	I/O multiplex pin select 20 (N/A, no multiplexed I/O in this set)
0x0861:165C	SYS_RESET	PIN_SEL_21	I/O multiplex pin select 21
End of Table 3-37			

Bits 31–8 of the 32-bit VBUSP address bus define the block location of the system reset controller (SYS_RESET) starting at 0x0861:1600 and ending at 0x0861:16FF. Address bits 7–0 are used to define each 32-bit-wide address location within the SYS_RESET block. The SYS_RESET block only uses address bits 6–0, thus, register addressing greater than 0x0861:167F allows aliased writes and reads of SYS_RESET registers in the range 0x0861:1600 to 0x0861:167F.

3.5.1 SYS_RESET (PIN_SEL)

Table 3-38 through Table 3-58 are detailed maps covering the memory range 0x0861:160C to 0x0861:165C, with bit descriptions in Table 3-59.

Table 3-38 SYS_RESET (PIN_SEL_1) Register

0x0861:160C																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL H4		N/A TERMINAL E1		N/A TERMINAL F3		N/A TERMINAL E2		N/A TERMINAL E3		N/A TERMINAL A2		SSP3 TERMINAL E4		SSP2 TERMINAL D2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SSP1 TERMINAL D1		SSP0 TERMINAL D3		N/A TERMINAL G4		N/A TERMINAL K9		N/A TERMINAL C2		N/A TERMINAL C1		N/A TERMINAL A1		N/A TERMINAL F4	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-39 SYS_RESET (PIN_SEL_2) Register

0x0861:1610																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL K2		N/A TERMINAL K3		N/A TERMINAL J1		N/A TERMINAL L11		N/A TERMINAL J2		N/A TERMINAL H1		N/A TERMINAL J4		N/A TERMINAL J3	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL H2		N/A TERMINAL G1		N/A TERMINAL H3		N/A TERMINAL G2		N/A TERMINAL B1		N/A TERMINAL F1		N/A TERMINAL G3		N/A TERMINAL F2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-40 SYS_RESET (PIN_SEL_3) Register

0x0861:1614																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL N4		N/A TERMINAL M11		N/A TERMINAL M3		N/A TERMINAL N1		N/A TERMINAL M1		N/A TERMINAL M9		N/A TERMINAL M2		N/A TERMINAL M4	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL L4		N/A TERMINAL L10		N/A TERMINAL L3		N/A TERMINAL L9		N/A TERMINAL K4		N/A TERMINAL L1		N/A TERMINAL L2		N/A TERMINAL K1	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-41 SYS_RESET (PIN_SEL_4) Register

0x0861:1618																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO03 TERMINAL T2		GPIO02 TERMINAL U3		GPIO01 TERMINAL T3		GPIO00 TERMINAL R3		N/A TERMINAL N11		N/A TERMINAL N9		N/A TERMINAL T1		N/A TERMINAL P9	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL R1		N/A TERMINAL M10		N/A TERMINAL R2		N/A TERMINAL P3		N/A TERMINAL P2		N/A TERMINAL P1		N/A TERMINAL N3		N/A TERMINAL N2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-42 SYS_RESET (PIN_SEL_5) Register

0x0861:161C																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL W7		N/A TERMINAL W3		N/A TERMINAL V3		N/A TERMINAL AB2		N/A TERMINAL T4		N/A TERMINAL V4		N/A TERMINAL U4		N/A TERMINAL R4	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL AB1		GPIO07 TERMINAL V1		GPIO06 TERMINAL U1		GPIO05 TERMINAL V2		GPIO04 TERMINAL U2		N/A TERMINAL N10		N/A TERMINAL P4		N/A TERMINAL P10	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-43 SYS_RESET (PIN_SEL_6) Register

0x0861:1620																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL Y6		N/A TERMINAL Y7		N/A TERMINAL AB5		N/A TERMINAL AA5		N/A TERMINAL Y5		N/A TERMINAL Y4		N/A TERMINAL AA4		N/A TERMINAL AA3	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL AB4		N/A TERMINAL AB3		N/A TERMINAL Y2		N/A TERMINAL W2		N/A TERMINAL Y1		N/A TERMINAL W1		N/A TERMINAL W4		N/A TERMINAL AA1	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-44 SYS_RESET (PIN_SEL_7) Register

0x0861:1624																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	KEYPAD07 TERMINAL Y9		KEYPAD06 TERMINAL AA9		KEYPAD05 TERMINAL AB9		N/A TERMINAL W9		KEYPAD04 TERMINAL Y8		KEYPAD03 TERMINAL AA8		KEYPAD02 TERMINAL AB8		KEYPAD01 TERMINAL AA7	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYPAD00 TERMINAL AB7		N/A TERMINAL AB6		N/A TERMINAL AA6		N/A TERMINAL Y3		N/A TERMINAL W6		N/A TERMINAL W8		N/A TERMINAL W5		N/A TERMINAL AA2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-45 SYS_RESET (PIN_SEL_8) Register

0x0861:1628																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LCD_PIXEL_STRB TERMINAL Y12		N/A TERMINAL W13		LCD_BIAS_E0 TERMINAL AA12		N/A TERMINAL P12		N/A TERMINAL M12		KEYPAD15 TERMINAL AB12		KEYPAD14 TERMINAL Y11		KEYPAD13 TERMINAL W11	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYPAD12 TERMINAL AA11		N/A TERMINAL P11		KEYPAD11 TERMINAL AB11		N/A TERMINAL W10		N/A TERMINAL L12		KEYPAD10 TERMINAL Y10		KEYPAD09 TERMINAL AA10		KEYPAD08 TERMINAL AB10	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-46 SYS_RESET (PIN_SEL_9) Register

0x0861:162C																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LCD_D09 TERMINAL Y16		LCD_D08 TERMINAL AA16		LCD_D07 TERMINAL AB16		LCD_D06 TERMINAL Y15		N/A TERMINAL N12		LCD_D05 TERMINAL AA15		LCD_D04 TERMINAL AB15		N/A TERMINAL W14	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCD_D03 TERMINAL Y14		LCD_D02 TERMINAL AA14		LCD_D01 TERMINAL AB14		LCD_D00 TERMINAL Y13		N/A TERMINAL M13		LCD_VSYNC_A TERMINAL AA13		$\overline{\text{LCD\_HSYNC\_W}}$ TERMINAL W12		LCD_E1 TERMINAL AB13	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-47 SYS_RESET (PIN_SEL_10) Register

0x0861:1630																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL AB21		$\overline{\text{P0\_FDUPLEX}}$ TERMINAL AA20		N/A TERMINAL P13		N/A TERMINAL W16		N/A TERMINAL K13		$\overline{\text{P0\_ACTIVITY}}$ TERMINAL AB20		$\overline{\text{P0\_LINK}}$ TERMINAL AA19		$\overline{\text{P0\_100MB}}$ TERMINAL AB19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LCD_D15 TERMINAL AA18		LCD_D14 TERMINAL AB18		LCD_D13 TERMINAL W17		LCD_D12 TERMINAL Y17		N/A TERMINAL N13		N/A TERMINAL W15		LCD_D11 TERMINAL AA17		LCD_D10 TERMINAL AB17	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-48 SYS_RESET (PIN_SEL_11) Register

0x0861:1634																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL W21		N/A TERMINAL U21		N/A TERMINAL V19		N/A TERMINAL W19		N/A TERMINAL Y19		N/A TERMINAL U20		N/A TERMINAL V20		N/A TERMINAL Y21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL W18		N/A TERMINAL Y18		N/A TERMINAL W20		N/A TERMINAL Y20		N/A TERMINAL Y22		N/A TERMINAL AA22		N/A TERMINAL AB22		N/A TERMINAL AA21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-49 SYS_RESET (PIN_SEL_12) Register

0x0861:1638																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL N14		N/A TERMINAL P20		N/A TERMINAL R20		N/A TERMINAL T20		N/A TERMINAL U19		N/A TERMINAL P19		N/A TERMINAL R19		N/A TERMINAL T19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL U22		N/A TERMINAL R21		N/A TERMINAL R22		N/A TERMINAL T22		N/A TERMINAL T21		N/A TERMINAL V21		N/A TERMINAL V22		N/A TERMINAL W22	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-50 SYS_RESET (PIN_SEL_13) Register

0x0861:163C																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TELE_RINGIN4 TERMINAL L22		TELE_RINGIN3 TERMINAL L21		TELE_RINGIN2 TERMINAL M22		TELE_RINGIN1 TERMINAL M21		N/A TERMINAL P14		N/A TERMINAL N19		TELE_CLK_I TERMINAL L19		TELE_DO TERMINAL M20	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TELE_DI TERMINAL N20		TELE_DCLK TERMINAL M19		N/A TERMINAL M14		N/A TERMINAL N22		N/A TERMINAL N21		N/A TERMINAL P22		N/A TERMINAL L13		N/A TERMINAL P21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-51 SYS_RESET (PIN_SEL_14) Register

0x0861:1640																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL G21		N/A TERMINAL G22		N/A TERMINAL H20		N/A TERMINAL J19		N/A TERMINAL H21		N/A TERMINAL H22		N/A TERMINAL J20		N/A TERMINAL J21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TELE_CLK_O TERMINAL J22		$\overline{\text{TELE\_RESET}}$ TERMINAL K22		N/A TERMINAL J14		TELE_INT TERMINAL K21		$\overline{\text{TELE\_CS}}$ TERMINAL K20		N/A TERMINAL L14		TELE_FS TERMINAL L20		N/A TERMINAL K19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-52 SYS_RESET (PIN_SEL_15) Register

0x0861:1644																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL D20		N/A TERMINAL D21		N/A TERMINAL D22		N/A TERMINAL K14		N/A TERMINAL E19		N/A TERMINAL E20		N/A TERMINAL C20		N/A TERMINAL E21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL E22		N/A TERMINAL H19		N/A TERMINAL F19		N/A TERMINAL F20		N/A TERMINAL F21		N/A TERMINAL F22		N/A TERMINAL G20		N/A TERMINAL D19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-53 SYS_RESET (PIN_SEL_16) Register

0x0861:1648																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL B22		N/A TERMINAL B18		N/A TERMINAL A18		N/A TERMINAL C18		N/A TERMINAL D18		N/A TERMINAL D16		N/A TERMINAL J13		N/A TERMINAL A19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL B19		N/A TERMINAL B21		N/A TERMINAL A20		N/A TERMINAL B20		N/A TERMINAL C19		N/A TERMINAL C21		N/A TERMINAL C22		N/A TERMINAL G19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-54 SYS_RESET (PIN_SEL_17) Register

0x0861:164C																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL A14		N/A TERMINAL D14		N/A TERMINAL A22		N/A TERMINAL C14		N/A TERMINAL B15		N/A TERMINAL A15		N/A TERMINAL C15		N/A TERMINAL B16	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL A16		N/A TERMINAL A21		N/A TERMINAL C16		N/A TERMINAL D15		N/A TERMINAL B17		N/A TERMINAL A17		N/A TERMINAL C17		N/A TERMINAL D17	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-55 SYS_RESET (PIN_SEL_18) Register

0x0861:1650																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL B11		N/A TERMINAL A11		N/A TERMINAL C11		N/A TERMINAL K11		N/A TERMINAL D11		N/A TERMINAL J12		N/A TERMINAL B12		N/A TERMINAL D13	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL A12		N/A TERMINAL C12		N/A TERMINAL K12		N/A TERMINAL D12		N/A TERMINAL B13		N/A TERMINAL A13		N/A TERMINAL C13		N/A TERMINAL B14	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-56 SYS_RESET (PIN_SEL_19) Register

0x0861:1654																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL B7		N/A TERMINAL C7		N/A TERMINAL A8		N/A TERMINAL D9		N/A TERMINAL B8		N/A TERMINAL J9		N/A TERMINAL C8		N/A TERMINAL A9	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL B9		N/A TERMINAL C9		N/A TERMINAL C10		N/A TERMINAL B10		N/A TERMINAL K10		N/A TERMINAL D10		N/A TERMINAL A10		N/A TERMINAL J11	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-57 SYS_RESET (PIN_SEL_20) Register

0x0861:1658																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	N/A TERMINAL B2		N/A TERMINAL C4		N/A TERMINAL B4		N/A TERMINAL B5		N/A TERMINAL C5		N/A TERMINAL A4		N/A TERMINAL A5		N/A TERMINAL C3	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A TERMINAL A6		N/A TERMINAL D8		N/A TERMINAL C6		N/A TERMINAL B6		N/A TERMINAL D5		N/A TERMINAL D6		N/A TERMINAL D4		N/A TERMINAL A7	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-58 SYS_RESET (PIN_SEL_21) Register

0x0861:165C																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								Test TERMINAL B3		N/A TERMINAL A3		N/A TERMINAL J10		N/A TERMINAL D7	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3-59 SYS_RESET (PIN_SEL_1 to PIN_SEL_21) Register Bits

Bit	Name	Description
31:8	PIN_SEL_21 only, reserved	Always returns zero when read
	PIN_SEL_21 to PIN_SEL_1, multiplex select	I/O multiplex pin select. All of the I/Os featuring multiple functional modes are shown in Table 3-3. This SYS_RESET (PIN_SEL_X) register set provides a 2-bit field for every I/O terminal, even though not all are useful. 11 = 3rd (tertiary) = Selects the tertiary multiplex feature 10 = 2nd (secondary) = Selects the secondary multiplex feature 01 = 1st (primary) = Selects the primary multiplex feature 00 = 3-state = POR mode: I/Os with multiple functional modes must be programmed to be useful. I/Os with multiple functional modes are identified in the registers listed in Table 3-38 to Table 3-58 with their primary (1st) mode name. N/A = Indicates terminal locations that do not have a multiplexed I/O feature. The 2-bit selection contents can be written to any binary state, but the I/O always remains at the primary (1st) selection function. Test-mode multiplex I/O features are selected through activation of the TEST terminal and override any other multiplex selection.
End of Table 3-59		

3.6 Pullup/Pulldown Configuration

The TNETV1056 provides the ability to power off any internal I/O terminal pullup or pulldown (see Table 3-3). This power-down feature is provided through the registers shown in Table 3-60.

Table 3-60 SYS_CLK (PULL_POWER) Register Set

Address	Block	Name	Description
0x0861:0A08	SYS_CLK	PULL_POWER_1	Pullup/pulldown power down 1
0x0861:0A10	SYS_CLK	PULL_POWER_2	Pullup/pulldown power down 2
0x0861:0A14	SYS_CLK	PULL_POWER_3	Pullup/pulldown power down 3
End of Table 3-60			

3.6.1 SYS_CLK (PULL_POWER)

Table 3-61 through Table 3-63 are detailed maps coving the memory range 0x0861:0A08 to 0x0861:0A14, with bit descriptions in Table 3-64.

Table 3-61 SYS_CLK (PULL_POWER_1) Register

0x0861:0A08								
Bit	31	30	29	28	27	26	25	24
Name	GPIO06 U1	GPIO05 V2	GPIO04 U2	GPIO03 T2	GPIO02 U3	GPIO01 T3	GPIO00 R3	McBSP_FS_TX P3
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	McBSP_FS_RX P2	McBSP_D_RX N3	McBSP_CLK_TX N2	McBSP_CLK_RX M3	N/A L3	VLYNQ5_CLK K3	JTAG_TMS J1	JTAG_TDI H1
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	JTAG_TCK J3	JTAG_TRST H2	JTAG_EMU1 G1	JTAG_EMU0 H3	EJTAG_TMS G2	EJTAG_TDI G3	EJTAG_TCK F2	$\overline{\text{EJTAG\_TRST1}}$ E1
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	$\overline{\text{EJTAG\_TRST0}}$ F3	$\overline{\text{EJTAG\_SYSRST}}$ E2	EJTAG_DINT E3	SSP3 E4	SSP2 D2	SSP1 D1	SSP0 D3	TEST F4
Reset	0	0	0	0	0	0	0	0

Table 3-62 SYS_CLK (PULL_POWER_2) Register

0x0861:0A10								
Bit	31	30	29	28	27	26	25	24
Name	N/A AB22	N/A AA21	N/A AB21	$\overline{\text{P0\_FDUPLEX}}$ AA20	$\overline{\text{P0\_ACTIVITY}}$ AB20	$\overline{\text{P0\_LINK}}$ AA19	$\overline{\text{P0\_100MB}}$ AB19	MULTI3
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	MULTI2	MULTI1	LCD_VSYNC_A AA13	$\overline{\text{LCD\_HSYNC\_W}}$ W12	LCD_E1 AB13	LCD_PIXEL_STRB Y12	LCD_BIAS_E0 AA12	KEYPAD15 AB12
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	KEYPAD14 Y11	KEYPAD13 W11	KEYPAD12 AA11	KEYPAD11 AB11	KEYPAD10 Y10	KEYPAD09 AA10	KEYPAD08 AB10	KEYPAD07 Y9
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	KEYPAD06 AA9	KEYPAD05 AB9	KEYPAD04 Y8	KEYPAD03 AA8	KEYPAD02 AB8	KEYPAD01 AA7	KEYPAD00 AB7	GPIO07 V1
Reset	0	0	0	0	0	0	0	0

Table 3-63 SYS_CLK (PULL_POWER_3) Register

0x0861:0A14								
Bit	31	30	29	28	27	26	25	24
Name	Nothing						MULTI10	MULTI9
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	MULTI8	UART_CTS B3	UART_RX B4	EM_HIZ C6	EM_WAIT B6	MULTI7	MULTI6	MULTI5
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	MULTI4	TELE_CLK_O J22	$\overline{\text{TELE\_RESET}}$ K22	TELE_INT K21	$\overline{\text{TELE\_CS}}$ K20	TELE_FS L20	TELE_RINGIN4 L22	TELE_RINGIN3 L21
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	TELE_RINGIN2 M22	TELE_RINGIN1 M21	TELE_CLK_I L19	TELE_DO M20	TELE_DI N20	TELE_DCLK M19	ALT_CLK_I P21	N/A AA22
Reset	0	0	0	0	0	0	0	0

Table 3-64 SYS_CLK (PULL_POWER) Register Bits

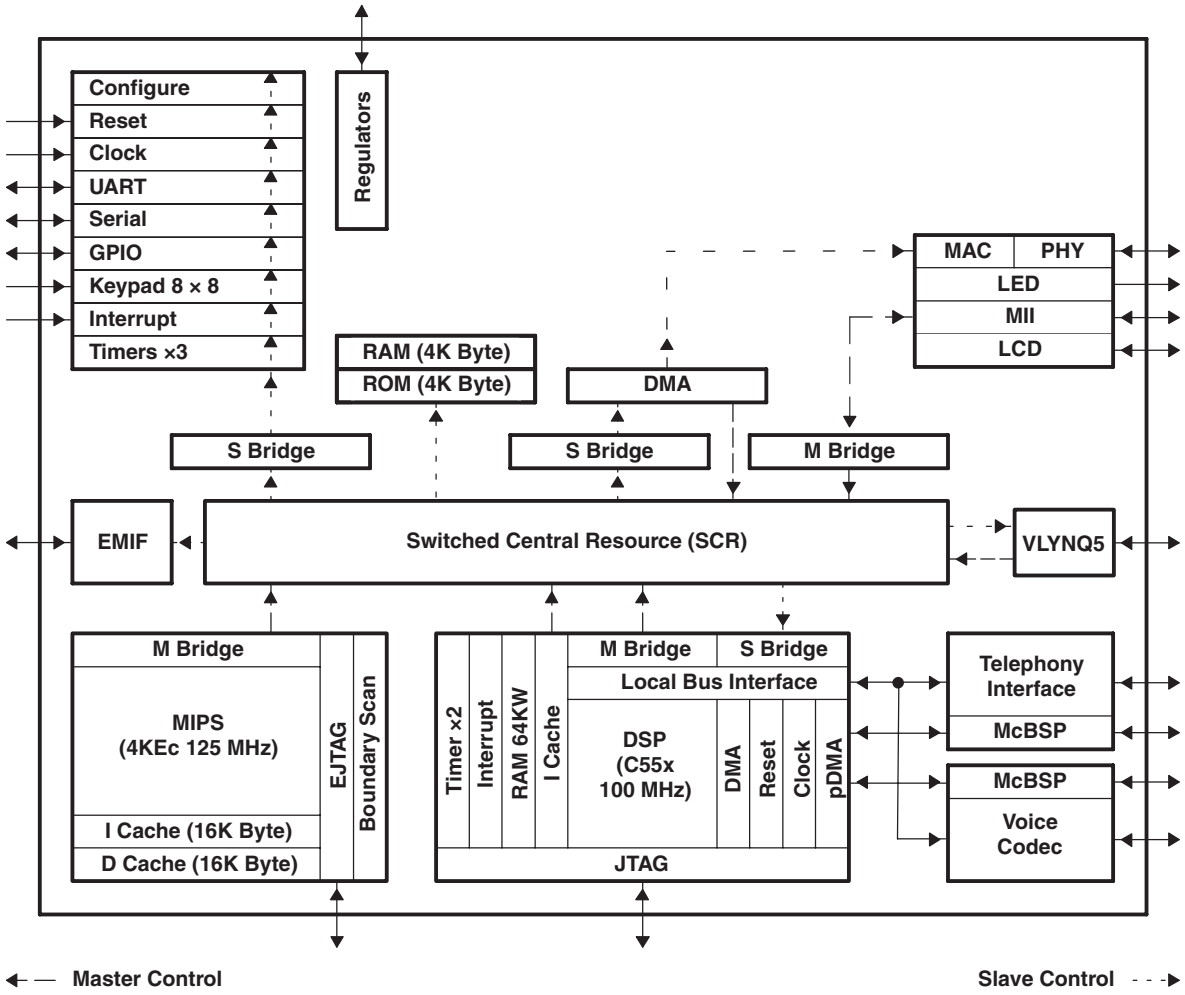
Bit	Name	Description
31:26	PULL_POWER_3, Nothing	May be written to any value, but values do nothing.
	PULL_POWER_3 to PULL_POWER_1, terminal number	Disable pullup/pulldown for the defined terminal 1 = Power off the pullup/pulldown 0 = Power on the pullup/pulldown The primary (1st) mode name is provided for all individual I/O locations. Multiple number locations are defined below.
	PULL_POWER_3 and PULL_POWER_2, multiple number	Disable pullup/pulldown for multiple terminals MULTI_10 = EM_A[23:16], terminals = D22, D21, D20, C22, C21, C19, B20, and A20 MULTI_9 = EM_A[15:8], terminals = F22, F21, F20, F19, E22, E21, E20, and E19 MULTI_8 = EM_A[7:0], terminals = J21, J20, H22, H21, H20, G22, G21, and G20 MULTI_7 = EM_D[31:24], terminals = A12, B12, D11, C11, A11, B11, A10, and B10 MULTI_6 = EM_D[23:16], terminals = C14, A14, B14, C13, A13, B13, D12, and C12 MULTI_5 = EM_D[15:8], terminals = A17, B17, C16, A16, B16, C15, A15, and B15 MULTI_4 = EM_D[7:0], terminals = B19, A19, D18, C18, A18, B18, D17, and C17 MULTI_3 = LCD_D[15:08], terminals = AA16, Y16, AB17, AA17, Y17, W17, AB18, and AA18 MULTI_2 = LCD_D[07:04], terminals = AB15, AA15, Y15, and AB16 MULTI_1 = LCD_D[03:01], terminals = Y13, AB14, AA14, and Y14
End of Table 3-64		

4 Functional Description

4.1 Block Diagram

The TNETV1056 functional block diagram shows the internal components discussed in this section (see Figure 4-1).

Figure 4-1 TNETV1056 Functional Block Diagram



Solid lines with arrow heads show the direction of data flow through the TNETV1056 subsystems. Master and Slave control are indicated by dotted lines, showing the direction of control through the switched central resource (SCR), rather than the direction of data flow.

The MIPS is always a master and the internal RAM is always a slave. Thus, read and write requests from the MIPS to the RAM generate a master control event at the SCR, while the RAM always responds to the SCR as a slave despite the direction of data flow.

4.2 Bus Structure

Data flow between TNETV1056 subsystems is conducted through the switched central resource (SCR). Those subsystems defined as master can request data reads or data writes from those subsystems defined as slave. As shown in Table 4-1, not all masters have access to all slaves. Table 4-1 shows a data path map for the SCR, identifying which masters can direct requests from which slaves (identified with a Y). In addition, the definition of bus types and bridges may be useful when using these subsystems.

Table 4-1 Internal Bus Structure

		Speed	VBUSP				VBUS		VBUSP
		Bridge	Y	Y	Y		South		
Speed	**Bridge**	**Masters / Slaves**	**MIPS**	**DSP I Cache**	**DSP**	**VLYNQ5**	**Ethernet**	**LCD**	**System DMA**
VBUSP	Y	**DSP**	Y			Y			Y
		VLYNQ5	Y				Y		Y
		ROM	Y						
		RAM	Y			Y			Y
		EMIF	Y	Y	Y	Y	Y		Y
VBUS	South	**Ethernet**	Y			Y			Y
		LCD							
		System Timers							
		UART							
		Serial							
		GPIO							
		Keypad							
VBUSP	West	**System DMA**	Y		Y	Y	Y		
		System Reset							
		System Clock							
		System Configure							
		System Interrupt							

The system SCR connects masters to slaves through bus segments. Each bus segment contains a 32-bit-wide data path capable of performing an entire data transfer in a single clock cycle. Two bus clock speeds are supported (VBUSP_CLK and VBUS_CLK). With a maximum VBUSP_CLK frequency of 125 MHz, the data bandwidth can reach 500 Mbytes per second (MBps) on a single bus segment. Because the SCR is a nonblocking architecture, simultaneous transactions are possible on different bus segments. A different bus segment is a command from a different master to a different slave. Arbitration is only required when two or more masters desire to access the same slave. Arbitration is a background round-robin task, eliminating any control overhead from reducing data bandwidth. The slaves have the ability to insert wait states before completing a data transfer.

An important component of the SCR is the bridge. Not all masters or slaves require a bridge, but those that do require it use the bridge to synchronize clocks, control signals, and bus protocol. In addition, certain bridges isolate a whole group of lower-performing peripherals into a single segment. The west slave bridge, south slave bridge, and south master bridge are all examples of grouped peripheral bridges. A slave bridge group constitutes a bus segment

end point, thus, only one slave in that group may be accessed in a single clock cycle SCR event. Likewise, a master bridge group constitutes a bus segment starting point and only one master in that group controls the SCR in a single clock cycle event. Arbitration for control of the SCR in the south master bridge is handled through an automated priority controller built into the bridge. This controller grants priority to the LCD first, then to the Ethernet.

All elements of the system bus structure (masters, slaves, bridges, and SCR) are hardwired without any software setup or control. As long as accesses are restricted to areas of the system memory map (as defined in the *TNETV1050 User's Guide*) used by the TNETV1056, this system bus performs as expected. If accesses are directed to unused areas of the system memory map, a system hang may occur. The hang is created by the SCR as it waits for the nonexistent slave to end wait state insertion. If this hang occurs, the TNETV1056 needs to be reset through the I/O signal $\overline{\text{RESET\_I}}$.

In addition to the system SCR, the DSP and Ethernet subsystems contain a local SCR. These local SCR bus units operate like the system SCR previously described. Most of the bus traffic on these local SCR units remains local, minimizing the DSP and Ethernet bandwidth on the system SCR. Through a master bridge, both of these local SCR bus units may gain master access to the system SCR. Through a slave bridge, system SCR master devices may control both of these local SCR bus units.

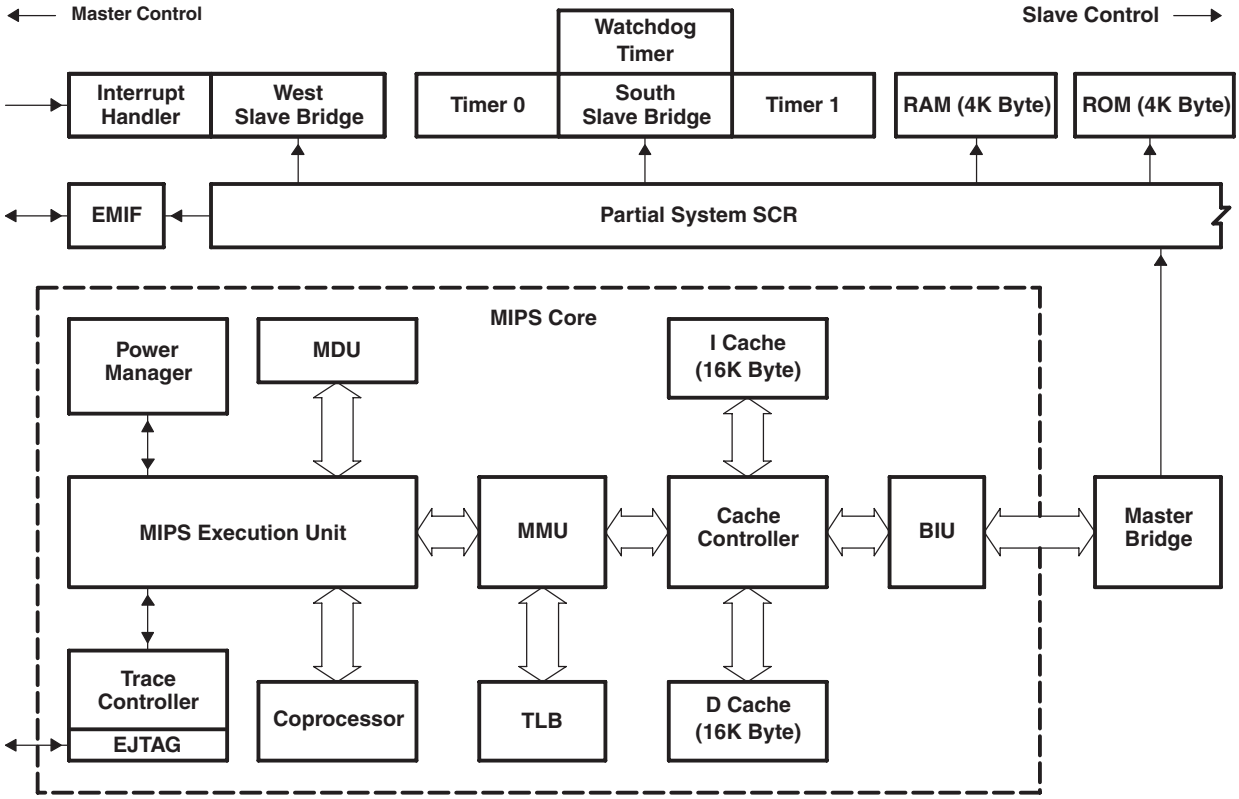
4.3 MIPS Subsystem

The MIPS subsystem (see Figure 4-2) consists of:

- MIPS32 4KEc 32-bit RISC processor with clock speeds up to 125 MHz
- 16K-byte four-way set-associative instruction cache (I cache)
- 16K-byte four-way set-associative data cache (D cache)
- Programmable MMU
- Enhanced JTAG (EJTAG) port
- 4K-byte RAM (zero wait state) accessed through the system SCR
- 4K-byte ROM (zero wait state) accessed through the system SCR
- Interrupt handler accessed through the system SCR
- Two universal 16-bit timers each with a 16-bit prescaled clock accessed through the system SCR
- One 16-bit watchdog timer with a 16-bit prescaled clock accessed through the system SCR

Details of the MIPS core, instruction cache, data cache, MMU, and EJTAG port may be found in the MIPS documentation identified in section 7 "Documentation Support" on page 166. The MIPS memory map and details of MIPS subsystem components not covered by the MIPS documentation may be found in the *TNETV1050 User's Guide*.

Figure 4-2 MIPS Block Diagram



4.3.1 Memory

The 4K-byte RAM may be used for either data variables or instructions.

The 4K-byte ROM is defined and loaded at the factory, containing just enough code to initialize and boot the TNETV1056 MIPS processor. Once initialized, the ROM directs the MIPS through the rest of the boot process as defined in section 3.4 "Boot Configuration" on page 60.

4.3.2 Interrupt Handler

One interrupt is presented to the MIPS from the TNETV1056 system. This interrupt is synthesized from 40 primary programmable-priority sources and 32 secondary fixed-priority sources. The interrupt source map is defined in the *TNETV1050 User's Guide*. Interrupt sources are individually programmable.

4.3.3 Universal Timers

Two universal 16-bit timers with programmable prescaled clocks are available for the MIPS. Each timer may be programmed for single-shot or auto-reload applications. An interrupt may be programmed to alert the MIPS when the timer count has expired.

4.3.4 Watchdog Timer

One 16-bit watchdog timer with a programmable prescaled clock is available for the MIPS. When the timer is programmed to run, the MIPS periodically must kick the watchdog timer. Kicking the watchdog timer prevents the timer count from expiring, thus preventing a system-initiated hardware reset.

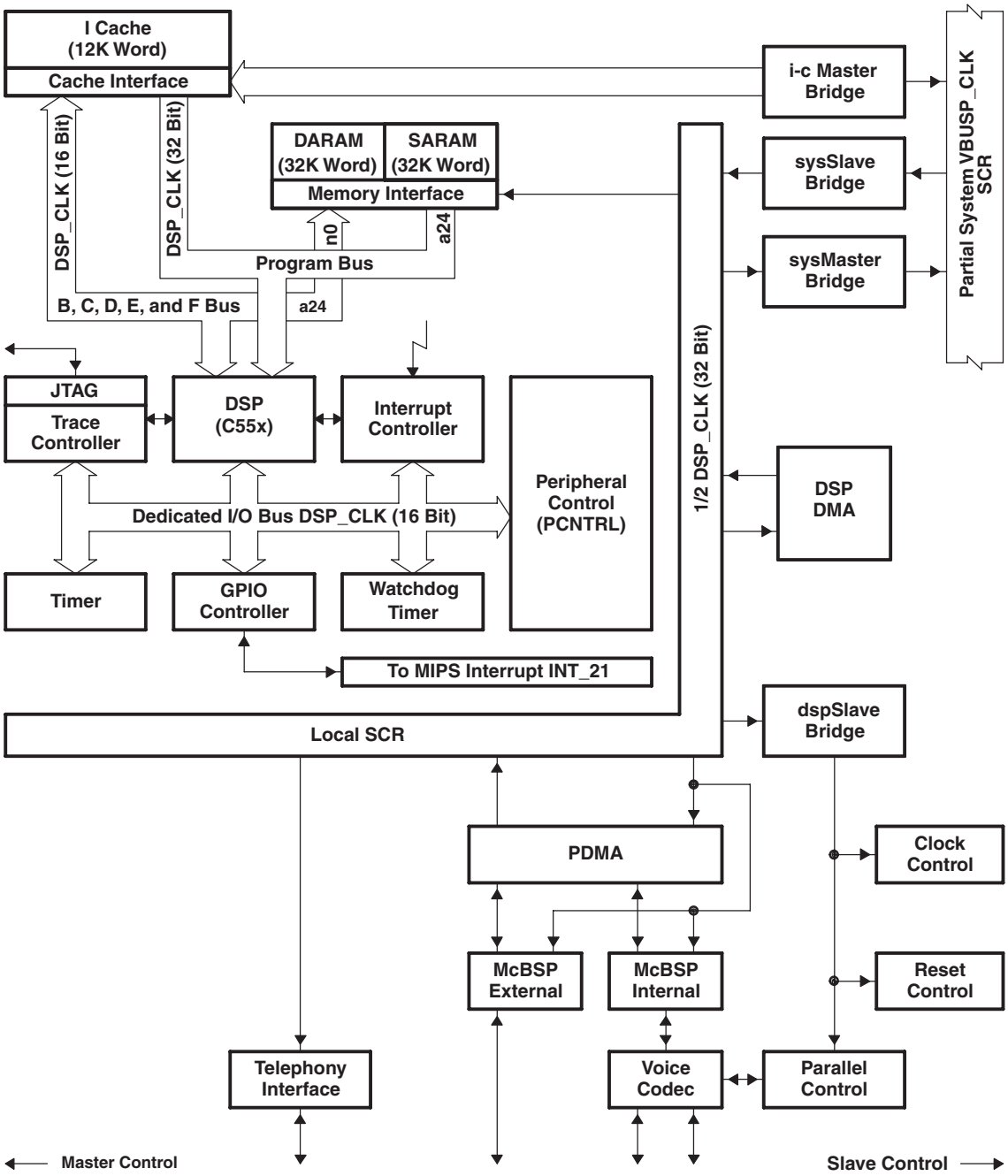
4.4 DSP Subsystem

The DSP subsystem (see Figure 4-3) consists of:

- C55x DSP with clock speeds up to 100 MHz
- JTAG port
- 12K-word two-way set associative instruction cache (I cache)
- 32K-word dual access RAM (DARAM) (zero wait state)
- 32K-word single access RAM (SARAM) (zero wait state)
- Interrupt handler
- 16-bit universal timer with prescaled clock
- 16-bit watchdog timer with prescaled clock
- Universal four-channel DMA controller
- Dedicated peripheral DMA controller

Details of the DSP and JTAG may be found in the DSP documentation identified in section 7 "Documentation Support" on page 166. The DSP memory map and details of DSP subsystem components not covered by the DSP documentation may be found in the *TNETV1050 User's Guide*.

Figure 4-3 DSP Block Diagram



4.5 Voice Codec Subsystem

The voice codec subsystem consists of the following elements:

- Dual-channel voice codec
- Analog crosspoint switch for input and output interface selection
- Multichannel buffered serial port (McBSP)
- 600-Ω telephone line interface

The on-chip voice codec is a highly integrated low-power high-performance dual-channel voice-frequency data converter. It features two 16-bit analog-to-digital (A/D) channels and two 16-bit digital-to-analog (D/A) channels. A programmable analog crosspoint switch allows the voice codec channels to be connected to various inputs and output devices, such as a handset, headset, speaker, microphone, or a 600-Ω telephone line interface.

The voice codec provides high-resolution signal conversion from digital to analog and from analog to digital using oversampling sigma-delta technology with programmable sampling rates.

The voice codec also integrates all the critical functions needed for most IP phone applications including a microphone preamplifier, handset amplifier, headset amplifier, 8-Ω speaker driver, programmable sidetone control, anti-aliasing filter (AAF), input/output programmable-gain amplifiers (PGA), and selectable low-pass IIR/FIR filters.

The voice codec implements extensive programmable power-management configurations including device power down and independent, per-channel, software control for turning off the ADC, DAC, op amps, and IIR/FIR filter (bypassable) to maximize system power conservation. The voice codec module consumes approximately 22 mW at 3.3 V with both channels enabled (not actively driving any analog outputs).

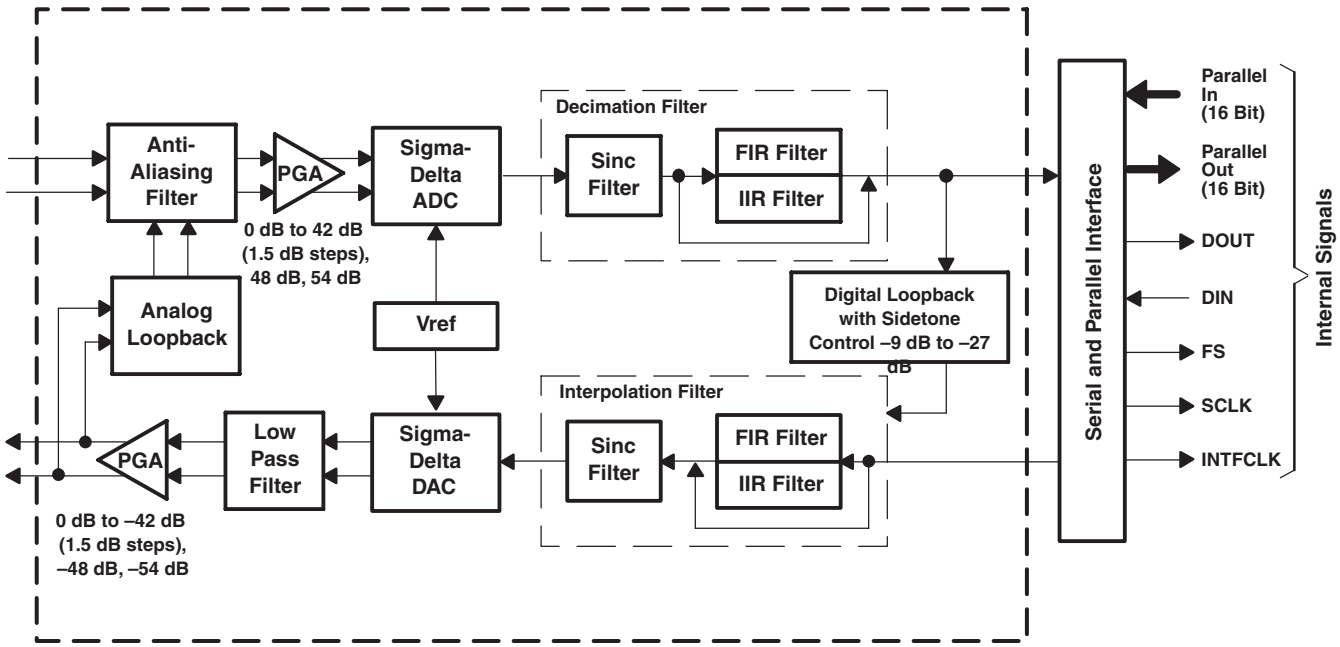
The McBSP interface provides a means to transmit and receive digital control and conversion data.

4.5.1 Features

- Two 16-bit oversampling sigma-delta ADCs
- Two 16-bit oversampling sigma-delta DACs
- Selectable IIR/FIR filter with bypassing option
- Programmable sampling rates:
  - 8 kHz or 16 kHz with on-chip IIR/FIR filter
  - 32 kHz and 64 kHz with IIR/FIR bypassed
- 81-dB SNR for ADC and 82-dB SNR for DAC
- G722-compliant ADC and DAC filters
- Turbo mode to maximize the bit clock for faster data transfer and higher data bandwidth
- Differential analog inputs, and differential and single-ended analog outputs
- Built-in analog functions:
  - analog and digital sidetone control
  - anti-aliasing filter (AAF)
  - programmable input and output gain control (PGA)
  - microphone/handset/headset amplifiers
  - 8-Ω speaker driver
- Separate software control for ADC and DAC power down
- Fully compatible with TI C5x DSP power supplies
  - 1.5-V digital core power
  - 3.3-V analog power
- Linear 2s-complement data format
- Test modes include digital loopback and analog loopback

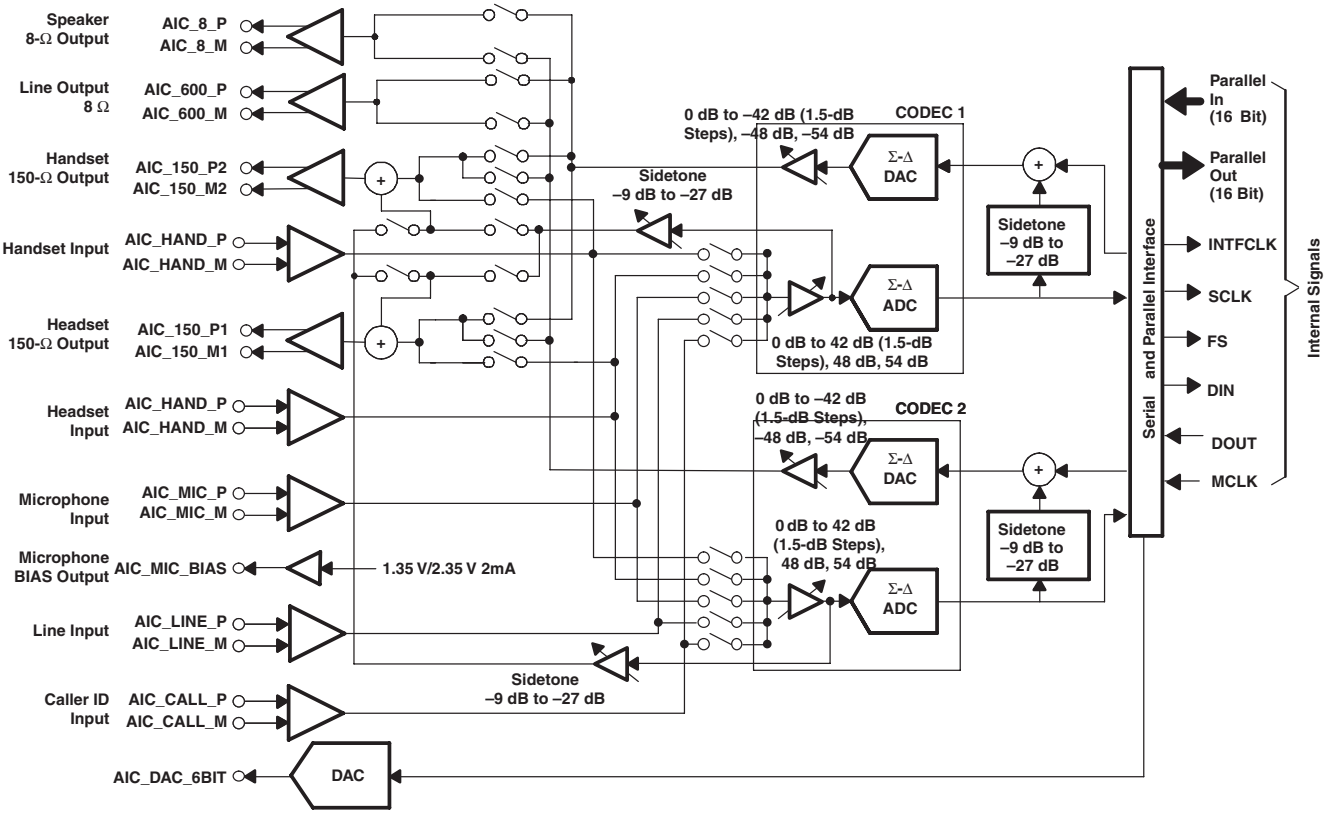
4.5.2 Functional Block Diagram (One of Two Channels Shown)

Figure 4-4 Voice Codec Functional Block Diagram



4.5.3 Functional Block Diagram

Figure 4-5 Voice Codec Subsystem Block Diagram



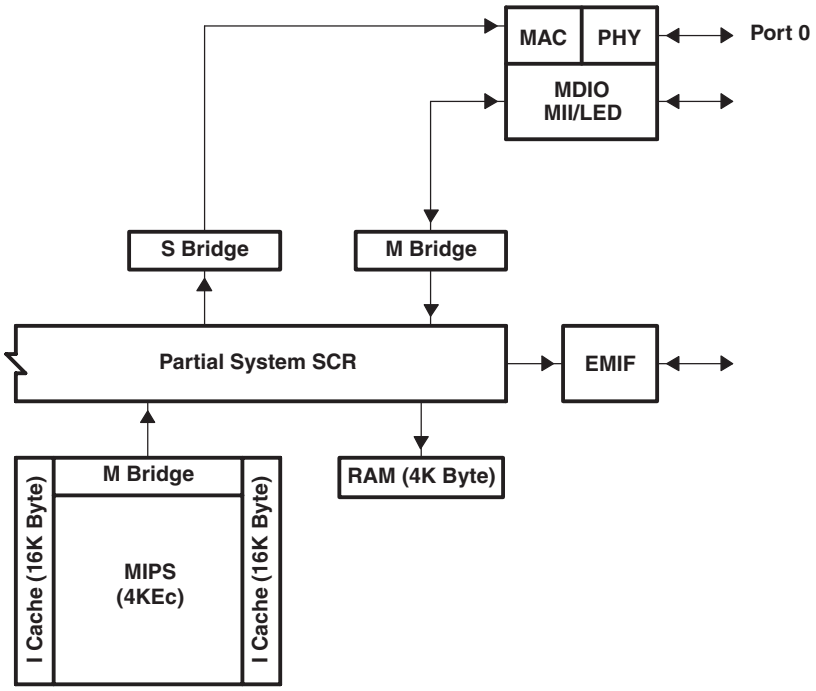
NOTE: The triangles following the input terminals on the left side of the above diagram do not represent real amplifiers. Instead, they show that these terminals are differential. The internal load presented to the terminals are resistors and switches. The internal blocks are all differential,but drawn as single-ended blocks for simplicity. If not used, these input terminals should be coupled to a quiet ground. The respective input paths should be configured as muted or off.

4.6 Ethernet Subsystem

The Ethernet subsystem (see Figure 4-6) consists of:

- One external Ethernet port that runs through an IEEE Std 802.3-compliant MAC and an IEEE Std 802.3/802.3u-compliant 10/100 Base-T PHY
- MIPS processor that initializes the subsystem and provides protocol support through the slave bridge
- EMIF that provides access to external memory (SDRAM) so the MAC control block can move DMA-received packets directly to SDRAM.

Figure 4-6 Ethernet Subsystem Block Diagram



4.7 Internal Voltage Regulator

TI recommends a 2.0-W supply for the 3.3-V (V_{DDS}) power rail and that the internal voltage regulator be used to produce the 1.5-V (V_{DD}) core voltage. This provides margin for the TNETV1056 to power up.

Two internal voltage regulators are required for the power consumption needs of the TNETV1056 V_{DD} (1.5-V) core voltage.

A top-view schematic (see Figure 4-7) shows the necessary external circuitry required to implement the TNETV1056 internal voltage regulator (see Table 4-2). In addition, the following guidelines should be followed when using the regulator:

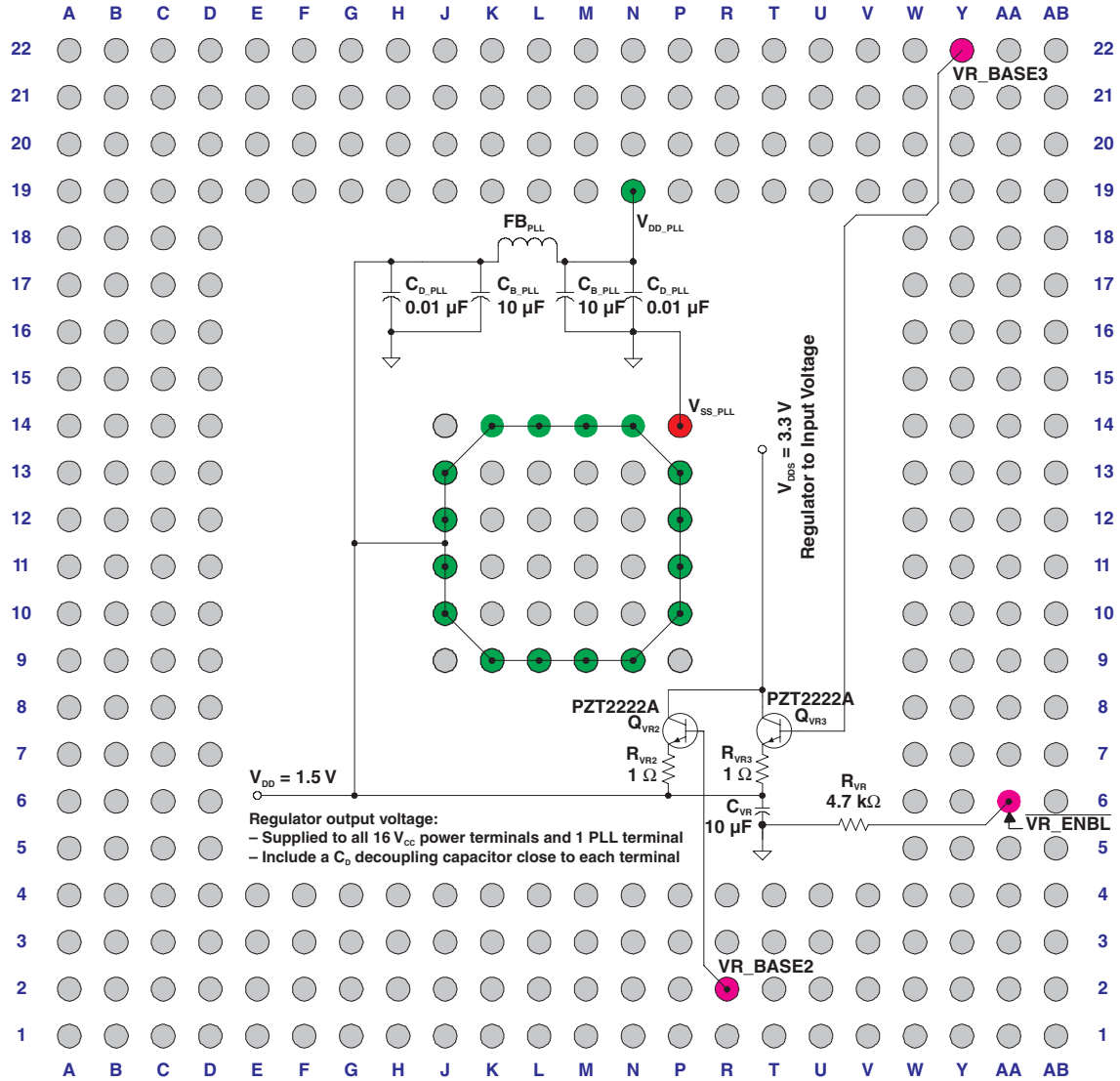
- The TNETV1056 V_{DD} (1.5-V) power rail may be created with this internal voltage regulator. Power provided from the V_{DDS} (3.3-V) power rail is regulated down to 1.5 V through two external pass transistors. The 1.5-V power produced by this internal voltage regulator provides power to all V_{DD} terminals (16 total), as well as the VDD_PLL terminal.
- To use the internal voltage regulator, it must be enabled by connecting the $\overline{\text{VR\_ENBL}}$ terminal to system ground (V_{SS}) through a pulldown resistor (R_{VR}).
- Each VR_BASE terminal is connected to the base of an external npn pass transistor (Q_{VR}).
  - Both transistors are required to produce the initial V_{DD} power-up supply current of 1.33 A total (2 W/1.5 V). Thus, each 1-Ω emitter resistor (R_{VR2}/R_{VR3}) momentarily provides a 0.67-V drop (1.33 A/2 × 1 Ω).
  - During normal operation, the 1-Ω emitter resistors each provide approximately a 0.18-V drop (0.36 A/2 × 1 Ω).
  - Lastly, a 10-µF tantalum capacitor (C_{VR}) must be used as shown in Figure 4-7.
- For best results, a separate split V_{DD} power plane should be created to route power to the TNETV1056. The 16 V_{DD} terminals have been placed conveniently in the center of the TNETV1056 to facilitate isolation for this split power plane.

- Decoupling capacitors (C_D) should be placed close to each V_{DD} terminal.

Table 4-2 Voltage Regulator Components

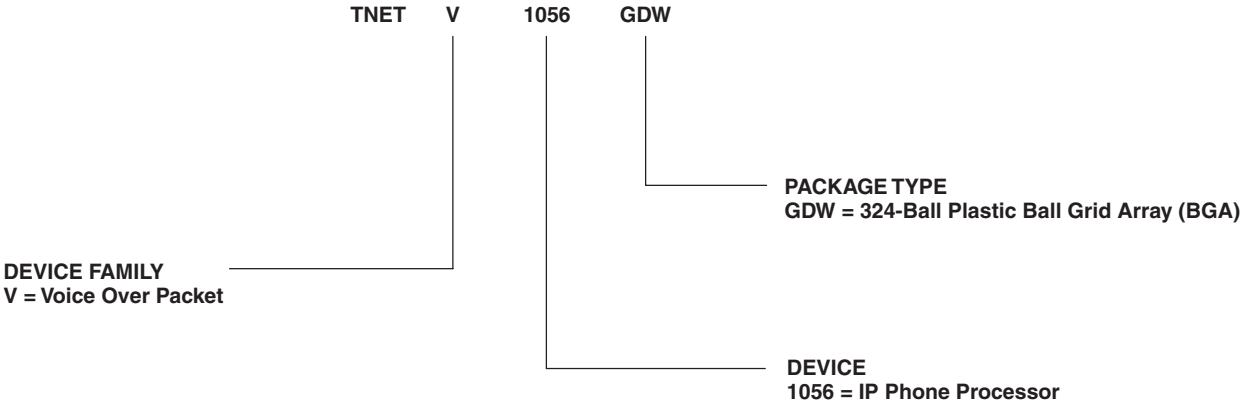
Item	Description	Value	Unit
Q_{VR2}	VR2 npn transistor	PZT2222A	
Q_{VR3}	VR3 npn transistor	PZT2222A	
C_{VR}	VR tantalum capacitor (±10%)	10	µF
R_{VR}	VR_ENBL pulldown resistor enabling the voltage regulator (±10%)	4.7	kΩ
R_{VR2}	VR2 emitter resistor (±5%), ¼ W	1	Ω
R_{VR3}	VR3 emitter resistor (±5%), ¼ W	1	Ω
C_D	V_{DD} 1.5-V decoupling capacitor	0.01	µF
V_{DDS}	Regulator input voltage	3.3	V
V_{DD}	Regulator output voltage	1.5	V

Figure 4-7 Voltage Regulator Schematic



4.8 TNETV1056 Device Nomenclature

Figure 4-8 TNETV1056 Device Nomenclature



5 Electrical Specification

This section provides the absolute maximum ratings, recommended operating conditions, electrical characteristics, timing requirements, and operating/switching characteristics for the TNETV1056 broadband communications processor.

All electrical and switching characteristics in this data manual are valid over the recommended operating conditions, unless otherwise specified.

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings (1)

Over operating free-air temperature range (unless otherwise noted)			
V_{DD}	Supply voltage range	Core logic	–0.5 V to 1.836 V
V_{DDS}		I/O	–0.5 V to 4 V
V_{DDA}		Analog, including codec and Ethernet PHY	–0.5 V to 3.6 V
V_I	Input voltage range	Except oscillator, analog voice codec, analog PHY, and voltage regulator	–0.5 V to 4.5 V
		Oscillator (AIC_CLK_I and REF_CLK_I)	–0.5 V to 2.336 V
		Analog PHY (PHY_REF)	–0.3 V to 3.6 V
		Voltage regulator ($\overline{\text{VR\_ENBL}}$)	–0.5 V to 4 V
V_O	Output voltage range	Except oscillator, analog voice codec, analog PHY, and voltage regulator	–0.3 V to V_{DDS}
		Analog voice codec differential (|AIC_8_P – AIC_8_M|)	2.8 V
		Analog PHY differential (|P0_TX_P – P0_TX_M|)	2.8 V
		Voltage regulator (VR_BASE2 and VR_BASE3)	–0.3 V to 1.52 V
T_J	Maximum junction temperature		105° C
T_{stg}	Storage temperature range		–65° C to 150° C
End of Table 5-1			

1 Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

Table 5-2 Recommended Operating Conditions

			Min	Nom	Max	Unit
V_{DD}	Supply voltage	Core logic	1.425	1.5	1.575	V
V_{DDS}		I/O	3.135	3.3	3.465	
V_{DDA}		Analog, including codec and Ethernet PHY	3.2	3.3	3.4	
V_{SS}	Supply ground		0			V
V_{IH}	High-level input voltage	Except oscillator, analog PHY, and voltage regulator	$0.7 \times V_{DDS}$		V_{DDS}	V
		Oscillator: AIC_CLK_I and REF_CLK_I	$0.7 \times V_{DD}$		1.575	
		Analog PHY, 10 Mbit: P0_RX_M, P0_RX_P			2.5	
		Analog PHY, 100 Mbit: P0_RX_M, P0_RX_P			1.3	
		Voltage regulator: $\overline{\text{VR\_ENBL}}$	2.5		3.6	
V_{IL}	Low-level input voltage	Except oscillator, analog voice codec, analog PHY, and voltage regulator	0		$0.3 \times V_{DDS}$	V
		Oscillator: AIC_CLK_I and REF_CLK_I	0		$0.3 \times V_{DD}$	
		Analog PHY, 10 Mbit: P0_RX_M, P0_RX_P	–2.5			
		Analog PHY, 100 Mbit: P0_RX_M, P0_RX_P	–1.3			
		Voltage regulator: $\overline{\text{VR\_ENBL}}$	0		0.9	
I_{OH}	High-level output current	All output terminals defined as 4mA in Table 3-3, Drive Current column			–4	mA
		All output terminals defined as 8 mA in Table 3-3, Drive Current column			–8	
I_{OL}	Low-level output current	All output terminals defined as 4 mA in Table 3-3, Drive Current column			4	mA
		All output terminals defined as 8 mA in Table 3-3, Drive Current column			8	
t_r	Rise time	10% to 90%, all clocks	0		5	ns
		10% to 90%, all other digital signal inputs not otherwise specified	0		25	
t_f	Fall time	90% to 10%, all clocks	0		5	ns
		90% to 10%, all other digital signal inputs not otherwise specified	0		25	
T_C	Temperature	Operating case temperature	0		70	°C
End of Table 5-2						

5.2.1 Electrical Characteristics

Electrical characteristics are over recommended ranges of supply voltage and operating case temperatures as defined in Table 5-3, unless otherwise noted.

Table 5-3 Electrical Characteristics (Part 1 of 2)

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{DI}	Differential input sensitivity	Analog voice codec: |AIC_CALL_P – AIC_CALL_M|, |AIC_HAND_P – AIC_HAND_M|, |AIC_HEAD_P – AIC_HEAD_M|, |AIC_LINE_P – AIC_LINE_M|, |AIC_MIC_P – AIC_MIC_M|, |AIC_8_P – AIC_8_M|		0		1.4	V
V_{OH}	High-level output voltage	Except oscillator, analog voice codec, analog PHY, and voltage regulator	I_{OH} = Max, V_{DDS} = 3.3 V	0.8 × V_{DDS}		V_{DDS}	V
		Oscillator: AIC_CLK_O and REF_CLK_O	I_{OH} = Max, V_{DD} = 1.3 V	0.8 × V_{DD}		1.65	
V_{OL}	Low-level output voltage	Except oscillator, analog voice codec, and analog PHY	I_{OL} = Max, V_{DD} = 3.3 V	0		0.22 × V_{DDS}	V
		Oscillator: AIC_CLK_O and REF_CLK_O	I_{OL} = Max, V_{DDS} = 1.3 V	0		0.22 × V_{DD}	
V_{DO}	Differential output voltage	Analog PHY, 10 Mbit: |P0_TX_P – P0_TX_M|		0		2.8	V
		Analog PHY, 100 Mbit: |P0_TX_P – P0_TX_M|		0		1.05	
		Analog voice codec: |AIC_8_P – AIC_8_M|		0		2	
I_I	Input current		V_{DD} = Max, V_I = V_{SS} to V_{DDS}			±10	µA
I_{OZ}	Off-state output current		V_O = V_{SS} to V_{DDS}			±10	µA
			No pullup/pulldown, driver disabled			±20	
			Pullup/pulldown active, driver disabled			±100	
C_i	Input capacitance					10	pF
C_o	Output capacitance					10	pF
P_{TOTAL}	Total power consumption	Total power consumption: With VOP call up running echo cancellation, driving an 8-Ω speaker, MIPS = 125 MHz, DSP = 100 MHz, using internal voltage regulator	V_{DD} = Max, V_{DDS} = Max, V_{DDA} = Max		1.4		W
I_{DDC}	Supply current (V_{DD}), core	Core logic supply only: MIPS = 125 MHz running Dhyrstone code benchmark application from SDRAM, DSP = 100 MHz running 75% dual MAC and 25% ADD code with moderate data bus activity (table of sine values) from the SDRAM. Excludes I/O and analog supplies.	V_{DD} = Max, V_{DDS} = Max, V_{DDA} = Max		360		mA
I_{DDS}	Supply current (V_{DDS}), I/O	I/O supply only: Supply for I/O ring	V_{DD} = Max, V_{DDS} = Max, V_{DDA} = Max		50		mA

Table 5-3 Electrical Characteristics (Part 2 of 2)

Parameter			Test Conditions	Min	Typ	Max	Unit
I_{DDA}	Supply current (V_{DDA}), analog Ethernet PHY	Ethernet subsystem only: Running 100-Mbit bidirectional full-duplex switch traffic with 64-byte frames at 75% utilization	V_{DD} = Max, V_{DDS} = Max, V_{DDA} = Max		85		mA
	Supply current (V_{DDA}), analog voice codec driving speaker	Telephony subsystem only: Receiving and echoing voice traffic at 16-kHz sampling rate, driving 8-Ω external speaker			135		
	Supply current (V_{DDA}), analog voice codec without driving speaker	Telephony subsystem only: Receiving and echoing voice traffic at 16-kHz sampling rate, not driving external speaker			8		
End of Table 5-3							

5.3 Package Thermal-Resistance Characteristics

Table 5-4 provides the thermal-resistance characteristics for the recommended package types used on the TNETV1056.

Table 5-4 Thermal Characteristics

Parameter		AIR FLOW (meters/s)	GDW/ZDW PACKAGE	Unit
$R_{\theta JA}$	Thermal resistance, junction to free air	0.0	22.5	°C/W
		0.5	21.1	
		1.0	20.3	
		2.0	19.5	
$R_{\theta JC}$	Thermal resistance, junction to case	NA	9.4	°C/W
$R_{\theta JB}$	Thermal resistance, junction to board	NA	14.0	°C/W
Ψ_{JT}	Thermal parameter, junction to package top	0.0	0.49	°C/W
		0.5	0.60	
		1.0	0.70	
		2.0	0.83	
End of Table 5-4				

5.4 Timing Parameter Symbol Definition

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, several of the terminal names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:

a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)

Letters and symbols and their meanings:

H	High
L	Low
I	Invalid
V	Valid
Z	High impedance
X	Unknown, changing, or don't care level

5.5 Clock Timing

This section provides the timing requirements and switching characteristics for the TNETV1056 clock network. For a complete view of the TNETV1056 clock structure, see Figure 3-5.

The TNETV1056 clock inputs include:

- REF_CLK (reference clock)—created with an internal oscillator that is driven by the two I/O signals REF_CLK_I and REF_CLK_O
- ALT_CLK (alternate clock)—created with the external clock that is supplied by the I/O signal ALT_CLK_I
- AIC_CLK (voice codec clock)—created with an internal oscillator that is driven by the two I/O signals AIC_CLK_I and AIC_CLK_O
- MIPS_PLL—output of the MIPS PLL subsystem, which may be fed back as an input to the other PLL units

The TNETV1056 produces the following internal clock sources from the previously defined clock inputs:

- MIPS_CLK (MIPS clock)—clock source for the MIPS subsystem
- MIPS_PLL (MIPS PLL subsystem output)—may be used to create the clock for any of the following internal clock sources
- DSP_CLK (DSP clock)—clock source for the DSP subsystem, also generates ½ DSP_CLK
- VBUSP_CLK (virtual bus pipeline clock)—clock source for all VBUSP subsystem peripherals and the switched central resource (SCR)
- VBUS_CLK (virtual bus clock)—clock source for all VBUS subsystem peripherals and the SCR
- PHY_CLK (Ethernet PHY clock)—clock source for the internal integrated Ethernet PHY subsystem. Upon entering the PHY subsystem, this clock encounters another PLL included in the PHY unit.
- AIC_CLK (voice codec clock)—clock source for the internal integrated voice codec subsystem. Can also source the MIPS and DSP clocks.
- LCD_CLK (liquid crystal display clock)—clock source for the LCD subsystem used for the driver circuitry

5.5.1 Internal Clock Speed Limits

As shown in Figure 3-5, there are many ways to produce the internal clocks. Regardless of the method of creation, the limits shown in Table 5-5 may not be exceeded.

Table 5-5 Internal Clock Speed Limits

	Description	Min	Typ	Max	Unit
MIPS_CLK	MIPS clock (1) (2)	1		125	MHz
DSP_CLK	DSP clock (1)	1		100	MHz
½ DSP_CLK	One-half DSP clock (1)	1		50	MHz
VBUSP_CLK	Virtual bus pipeline clock (1)	1		125	MHz
VBUS_CLK	Virtual bus clock (1) (3)	1		62.5	MHz
PHY_CLK	Ethernet PHY clock (may be 25 MHz or 50 MHz)	24.75	25	50	MHz
AIC_CLK	Voice codec clock	4.096	8.192	16.384	MHz
LCD_CLK	Liquid-crystal display clock	1		62.5	MHz
End of Table 5-5					

1 Specified by design
2 Standard PLL configuration supports 162.5-MHz MIPs clock maximum.
3 Standard PLL configuration supports 81.25-MHz VBUS clock maximum.

5.5.2 Reference Clock (REF_CLK)

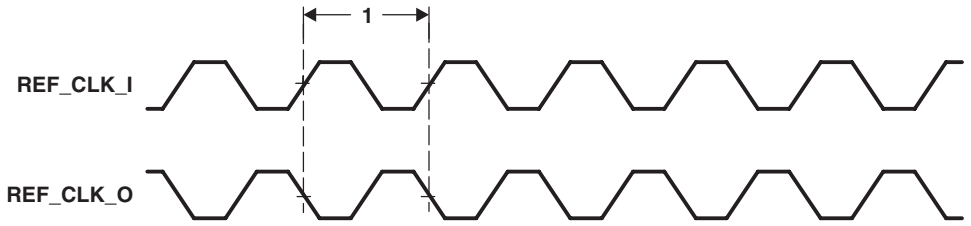
The reference clock is derived from an internal oscillator circuit driven from REF_CLK_I and REF_CLK_O (see Table 5-6). Use the following timing values when selecting an external crystal and refer to the*TNETV1050 User's Guide*, for more information.

Table 5-6 Reference Clock Timing

See Figure 5-1						
No.	**Description**		**Min**	**Typ**	**Max**	**Unit**
	$f_{clock(REF\_CLK)}$	Clock frequency, REF_CLK (1)	20	25	35	MHz
1	$t_{c(REF\_CLK)}$	Cycle time, REF_CLK	28.57	40	50	ns
	$f_{s(REF\_CLK)}$	Frequency stability, REF_CLK	–50		50	ppm
End of Table 5-6						

1 Specified by design

Figure 5-1 Reference Clock Input



5.5.3 Voice Codec Clock (AIC_CLK)

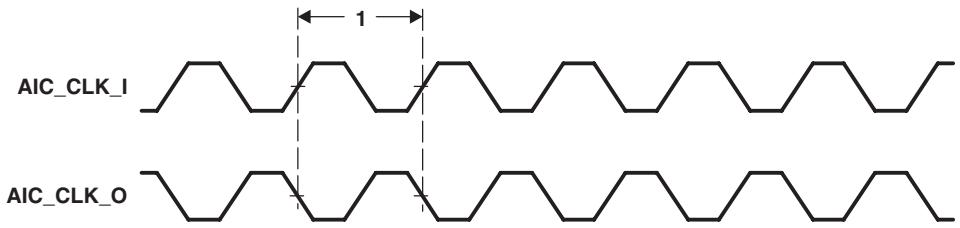
The voice codec clock is derived from an internal oscillator circuit driven from AIC_CLK_I and AIC_CLK_O (see Table 5-7).

Table 5-7 Voice Codec Clock Timing

See Figure 5-2						
No.	**Description**		**Min**	**Typ**	**Max**	**Unit**
		Clock frequency, AIC_CLK (1)	1	8.1920	20	MHz
1	$t_{c(AIC\_CLK)}$	Cycle time, AIC_CLK (1)	50	122.07	1000	ns
	$f_{s(AIC\_CLK)}$	Frequency stability, AIC_CLK (1)	–50		50	ppm
End of Table 5-7						

1 Specified by design. When AIC_CLK is input to the analog PLL, the analog PLL timing requirements in Table 5-9 must be met.

Figure 5-2 Voice Codec Clock



5.5.4 Alternate Clock (ALT_CLK)

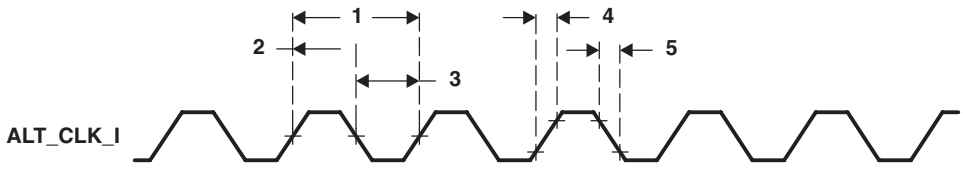
The alternate clock is derived from the ALT_CLK_I external clock source and has input timing shown in Table 5-8.

Table 5-8 Alternate Clock Timing

See Figure 5-3						
No.	**Description**		**Min**	**Typ**	**Max**	**Unit**
	$f_{clock(ALT\_CLK)}$	Clock frequency, ALT_CLK (1)	10	25	100	MHz
1	$t_{c(ALT\_CLK)}$	Cycle time, ALT_CLK (1)	10	A	100	ns
2	$t_{w(ALT\_CLK-H)}$	Pulse duration, ALT_CLK high (1)	A – 1	A/2	A + 1	ns
3	$t_{w(ALT\_CLK-L)}$	Pulse duration, ALT_CLK low (1)	A – 1	A/2	A + 1	ns
		Duty cycle, ALT_CLK (1)	40	50	60	%
4	$t_{r(ALT\_CLK)}$	Rise time, ALT_CLK (1)			5	ns
5	$t_{f(ALT\_CLK)}$	Fall time, ALT_CLK (1)			5	ns
End of Table 5-8						

1 Specified by design

Figure 5-3 Alternate Clock



5.5.5 Analog PLL

Within the TNETV1056 there are four identical analog PLL units, each with the timing values shown in Table 5-9.

Table 5-9 Analog PLL Unit Timing

See Figure 5-4 and Figure 5-5					
No.	**Description**		**Min**	**Max**	**Unit**
	$f_{clock(PLL\_IN)}$	Clock frequency, analog PLL_IN	10	100	MHz
1	$t_{c(PLL\_IN)}$	Cycle time, analog PLL_IN	10	100	ns
	$f_{clock(PLL\_OUT)}$	Clock frequency, analog PLL_OUT	10	250	MHz
2	$t_{c(PLL\_OUT)}$	Cycle time, analog PLL_OUT	4	100	ns
3	$t_{d(PLL\_REG)}$	Delay time, #_CLK_CTRL valid to PLL_OUT valid (1)		50	µs
End of Table 5-9					

1 Specified by design

Figure 5-4 Analog PLL

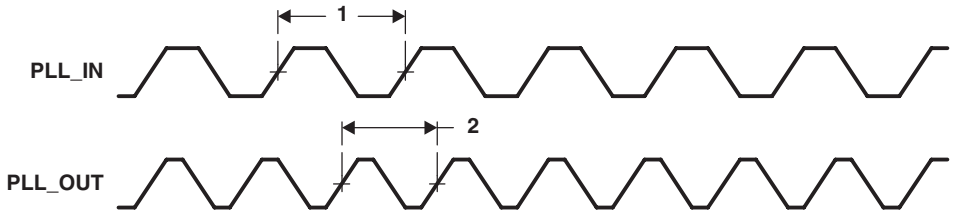
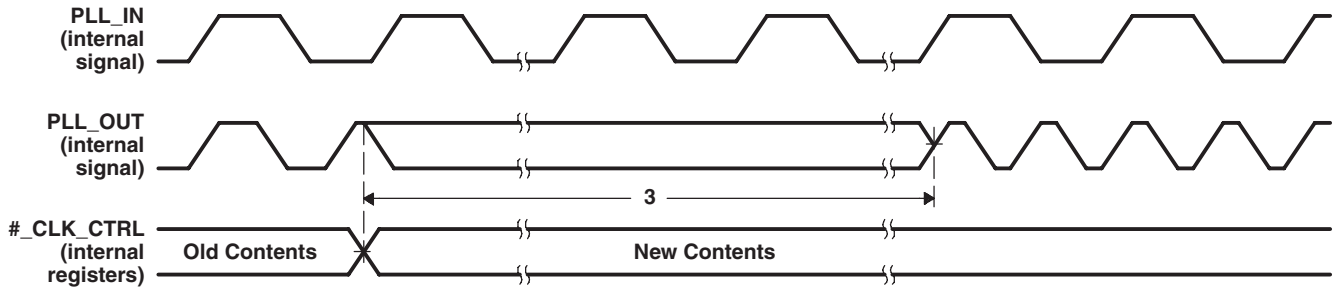


Figure 5-5 Analog PLL-OUT Transitory



5.5.6 PHY PLL

The PHY PLL takes an internal 25-MHz clock and generates the Ethernet PHY reference 20-MHz or 125-MHz clocks, respectively, for the 10 Base-T or 100 Base-T operating modes. From a hardware or software reset, the internal logic gives the PHY PLL approximately 256 µs to allow for PHY PLL stabilization. IEEE Std 802.3u, Clause 22 (22.2.4.1.1), states that the reset process should be completed within 0.5 s from initiation of the reset signal.

5.6 System Reset Timing

There are two kinds of reset events within the TNETV1056 (see Table 5-10):

- Power-on reset
- Hardware reset: Produced when either one of the following external input signals is forced to a low state:
  - $\overline{\text{RESET\_I}}$
  - $\overline{\text{EJTAG\_SYSRST}}$

Table 5-10 System Reset Timing

See Figure 5-6 and Figure 5-7

No.		Description	Min	Typ	Max	Unit
1	$t_{d(XTAL\_LOCK)}$	Delay time, $\overline{\text{RESET\_I}}\downarrow$ to PLL_IN valid (1) (The external crystal oscillator dictates this parameter.)		10		ms
2	$t_{d(BOOT\_POR)}$ (2)	Delay time, PLL_IN valid to $\overline{\text{RESET\_I}}$ invalid (3)	50			µs
3	$t_{d(BOOT\_HDW)}$ (2)	Delay time, PLL_IN valid to $\overline{\text{RESET\_I}}$ invalid (3)	$4 \times t_C$ (4)			ns
4	$t_{d(BOOT)}$ (2)	Delay time, $\overline{\text{RESET\_I}}$ to EM_A[23:00] invalid (3)			10	ns
5	$t_{h(BOOT)}$ (2)	Hold time, $\overline{\text{RESET\_I}}$ to EM_A[23:00] valid (3)	0			ns
6	$t_{d(MUX\_POR)}$	Delay time, multiplexed I/O (5) 3-state to $\overline{\text{RESET\_I}}/\overline{\text{EJAG\_SYSRST}}\uparrow$ (3)	$4 \times t_C$ (4)			ns
7	$t_{d(MUX\_SET\_HDW)}$ (2)	Delay time, $\overline{\text{RESET\_I}}/\overline{\text{EJAG\_SYSRST}}\uparrow$ to multiplexed I/O (5) valid (3)	50			µs
8	$t_{d(RSTOUT\_OFF\_HDW)}$	Delay time, $\overline{\text{RESET\_I}}/\overline{\text{EJAG\_SYSRST}}\uparrow$ to $\overline{\text{RESET\_O}}/\overline{\text{TELE\_RESET}}\uparrow$ (3) (6)	50			µs
9	$t_{w(HDW\_RESET)}$	Pulse width, $\overline{\text{RESET\_I}}/\overline{\text{EJAG\_SYSRST}}$ low (3)	$64 \times t_C$ (4)			ns
10	$t_{d(PLL\_CHANGE)}$	Delay time, PLL_OUT invalid to PLL_OUT valid (7)		50		µs

End of Table 5-10

1 PLL_IN: Represents the input source clock for all four internal analog PLL units shown in Figure 3-5. These clocks are not visible externally.

2 Boot configuration: The EMIF address bus (EM_A[23:00]) changes from an output to an input when a hardware reset is active. The TNETV1056 holds the latched input when the hardware reset goes inactive. As shown in section 3.4 "Boot Configuration" on page 60, the values of the boot configuration define the internal analog PLL inputs and outputs.

3 Specified by design

4 t_C = clock cycle time of PLL_IN

5 Multiplexed I/O: On hardware reset events, the multiplexed I/O transition to 3-state mode. After the reset event, these multiplexed I/O require software reprogramming to become useful. For more information related to the multiplexed I/O, see section 3.5 "Multiplex Configuration" on page 67.

6 Two reset output signals ($\overline{\text{RESET\_O}}$ and $\overline{\text{TELE\_RESET}}$) exit the TNETV1056. On both hardware and software reset events, both of these output signals are forced to an active low state. After the reset event, these external resets can be individually deactivated through software manipulation of registers in the SYS_RESET and DSP_RESET subsystems.

7 PLL_OUT: Represents the output of all four internal analog PLL units shown in Figure 3-5. On hardware reset events, each analog PLL unit transitions to an active PLL mode, with the VCO running and the output defined as $f_{PLL\_OUT} = (1 \times f_{PLL\_IN})$. These clocks are not visible externally.

Figure 5-6 Power-On Reset

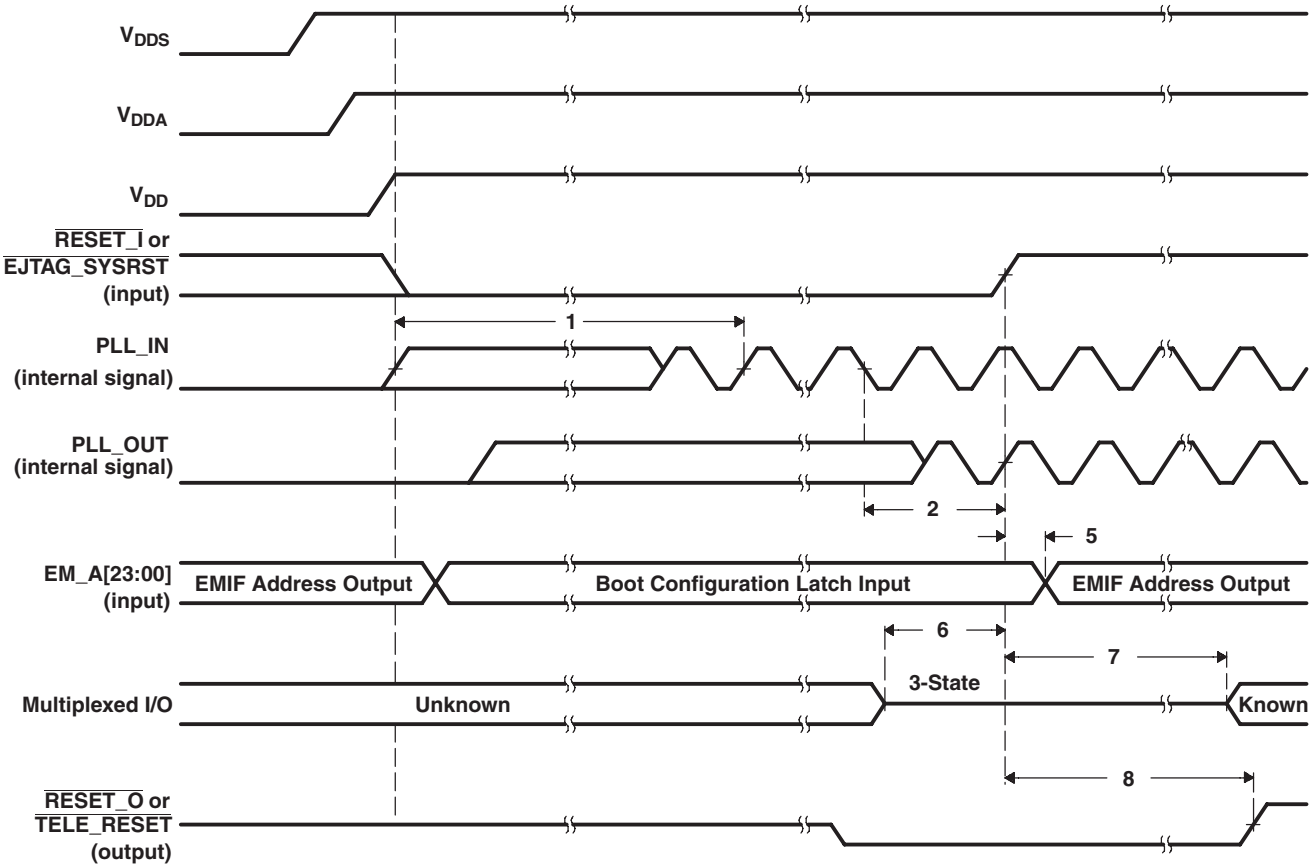
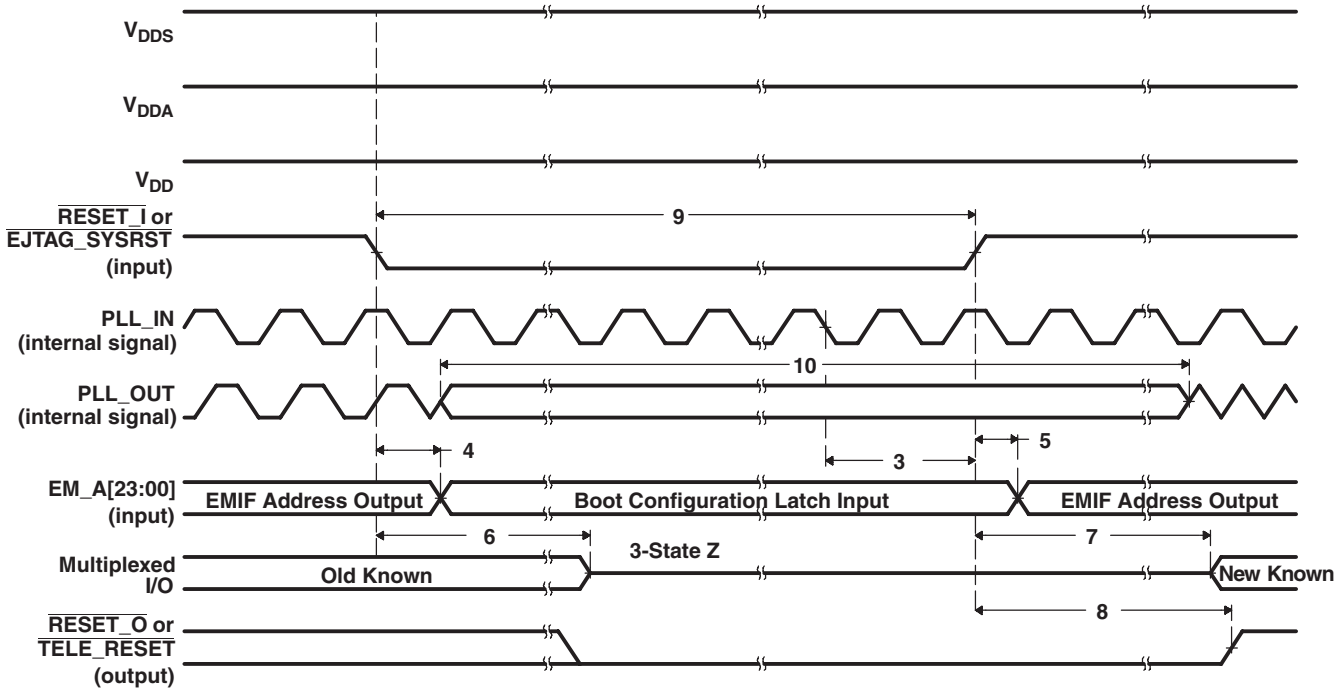


Figure 5-7 Hardware Reset



5.7 EMIF Timing

The EMIF shares several I/O signals, providing access to external SDRAM devices, as well as external asynchronous memory devices (see Table 5-11).

5.7.1 EMIF SDRAM

Table 5-11 EMIF SDRAM Timing

See Figure 5-8 and Figure 5-9					
No.	**Description**		**Min**	**Max**	**Unit**
	$f_{c(SDRAM\_CLK)}$	Frequency, EM_CLK		125	MHz
1	$t_{c(SDRAM\_CLK)}$	Cycle time, EM_CLK	8		ns
2	$t_{w(SDRAM\_CLK\_H)}$	Pulse duration, EM_CLK high	4		ns
3	$t_{w(SDRAM\_CLK\_L)}$	Pulse duration, EM_CLK low	3.4		ns
4	$t_{d(CMD\_V)}$	Delay time, EM_CLK high to command valid	1.2	5.5	ns
5	$t_{d(CMD\_I)}$	Delay time, EM_CLK high to command invalid	1.2	5.5	ns
6	$t_{d(ROW\_V)}$	Delay time, EM_CLK high to EM_A[12:00] row valid	1.2	5.5	ns
7	$t_{d(ROW\_I)}$	Delay time, EM_CLK high to EM_A[12:00] row invalid	1.2	5.5	ns
8	$t_{d(BANK\_V)}$	Delay time, EM_CLK high to EM_A[23:22] bank valid	1.2	5.5	ns
9	$t_{d(BANK\_I)}$	Delay time, EM_CLK high to EM_A[23:22] bank invalid	1.2	5.5	ns
10	$t_{d(DQM\_V)}$	Delay time, EM_CLK high to $\overline{\text{EM\_WE\_DQM[3:0]}}$ valid	1.2	5.5	ns
11	$t_{d(DQM\_I)}$	Delay time, EM_CLK high to $\overline{\text{EM\_WE\_DQM[3:0]}}$ invalid	1.2	5.5	ns
12	$t_{d(COLUMN\_V)}$	Delay time, EM_CLK high to EM_A[12:00] column valid	1.2	5.5	ns
13	$t_{d(COLUMN\_I)}$	Delay time, EM_CLK high to EM_A[12:00] column invalid	1.2	5.5	ns
14	$t_{d(WR\_DATA\_V)}$	Delay time, EM_CLK high to EM_D[31:00] valid	1	5.5	ns
15	$t_{d(WR\_DATA\_I)}$	Delay time, EM_CLK high to EM_D[31:00] invalid	1.2	5.5	ns
16	$t_{d(RD\_DATA)}$	Delay time, EM_D[31:00] valid to EM_CLK high	2		ns
17	$t_{d(RD\_DATA)}$	Delay time, EM_CLK high to EM_D[31:00] invalid	1.2		ns
18	$t_{d(BUS\_Z)}$	Delay time, EM_CLK high to EM_D[31:00] Z (3-state valid)		6.5	ns
19	$t_{d(Z\_BUS)}$	Delay time, EM_CLK high to EM_D[31:00] Z (3-state invalid)		6.5	ns
End of Table 5-11					

The SDRAM command is made up from several EMIF I/O signals as defined in Table 5-12.

Table 5-12 EMIF SDRAM Commands

Command	EM_CS2	EM_CS1	EM_RAS	EM_CAS	EM_WE	EM_WE_DQM3	EM_WE_DQM2	EM_WE_DQM1	EM_WE_DQM0	EM_A [12:00]	EM_A [23:22]	EM_CKE
COMMAND INHIBIT The SDRAM is deselected.	H	H	X	X	X	X	X	X	X	X	X	H
NOP No operation, although read and write bursts may be in progress.	H	L	H	H	H	X	X	X	X	X	X	H
	L	H										
ACTIVE Activate a row in a particular bank.	H	L	L	H	H	X	X	X	X	row	bank	H
	L	H										
READ Initiate a burst read access from an active row. The first data is returned after the CAS latency is exhausted. Data continues on subsequent clock cycles until the burst is exhausted or a BURST TERMINATE extinguishes the process.	H	L	H	L	H	L = EM_D [31:24]	L = EM_D [23:16]	L = EM_D [15:08]	L = EM_D [7:0]	column	bank	H
	L	H										
WRITE Initiate a burst write access to an active row. The first data is presented on the WRITE command. Data continues on subsequent clock cycles until the burst is exhausted or a BURST TERMINATE extinguishes the process.	H	L	L	H	H	L = EM_D [31:24]	L = EM_D [23:16]	L = EM_D [15:08]	L = EM_D [7:0]	column	bank	H
	L	H										
BURST TERMINATE Used to terminate the most recently registered fixed-length or full-page (read or write) burst.	H	L	H	H	L	X	X	X	X	X	X	H
	L	H										
PRECHARGE Deactivate the open row in a particular bank or the open row in all banks. Use the code to select the bank or all banks.	H	L	L	H	L	X	X	X	X	code	code	H
	L	H										
AUTO REFRESH Force a refresh to a row. Defined by register EMIF (SDRAM_REFRESH_CTRL)	L	L	L	L	H	X	X	X	X	X	X	H
SELF REFRESH Force the SDRAM into the internally generated refresh mode.	L	L	L	L	H	X	X	X	X	X	X	L
LOAD MODE REGISTER SDRAM operating mode written after initialization. Defined by register EMIF (SDRAM_CONFIG_CS_1_2).	L	L	L	L	L	X	X	X	X	op code	X	H
End of Table 5-12												

The LOAD MODE REGISTER portion of the SDRAM initialization procedure determines the CAS latency timing and the burst length. These parameters are programmable and provided in the EMIF (SDRAM_CONFIG_CS_1_2) register.

The following SDRAM command timing parameters are programmable through the EMIF (SDRAM_TIME_CTRL) register:

- TIME_RP
- TIME_RCD
- TIME_WR
- TIME_RAS
- TIME_RC
- TIME_RRD
- TIME_RFC

Figure 5-8 EMIF SDRAM Write

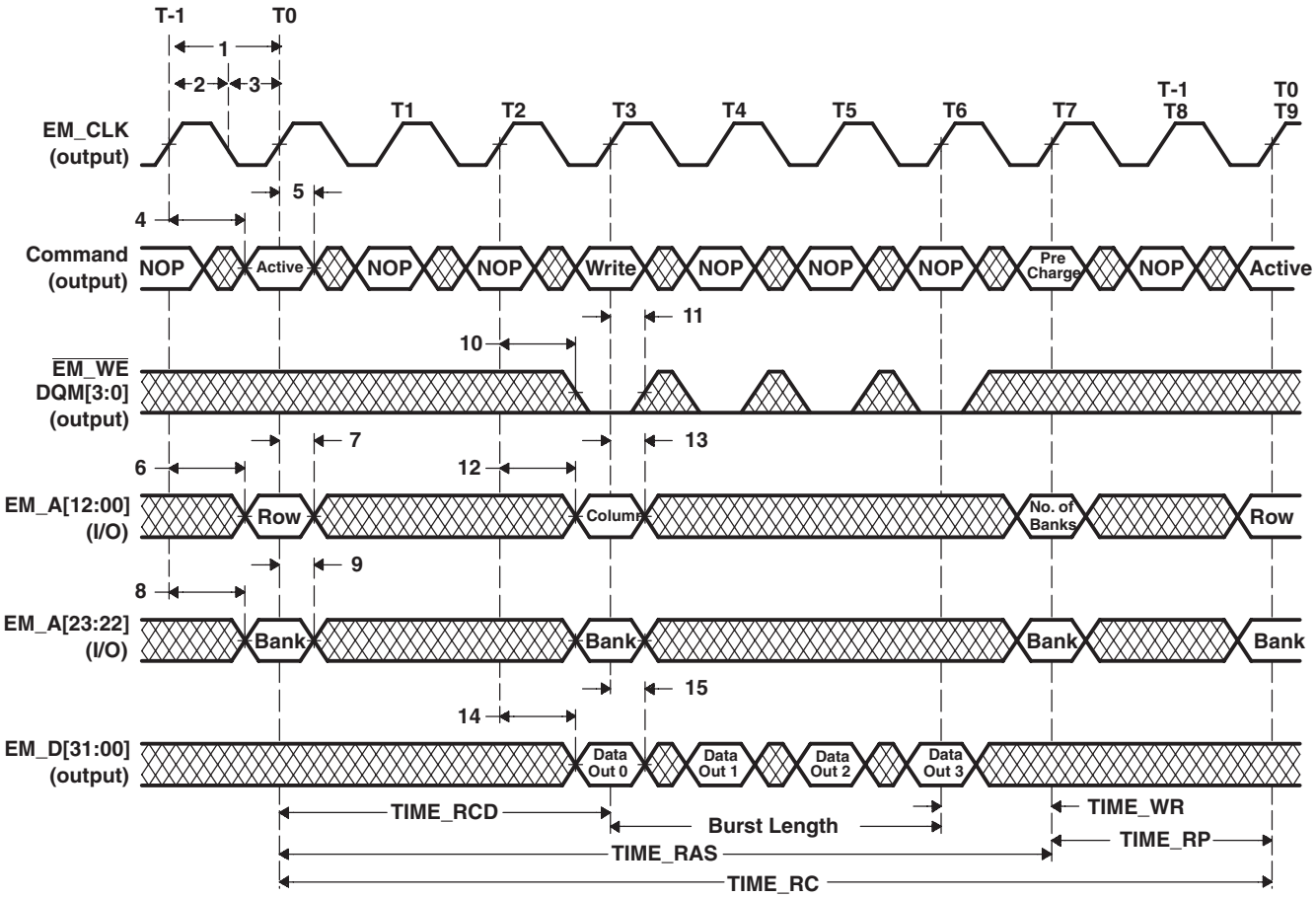
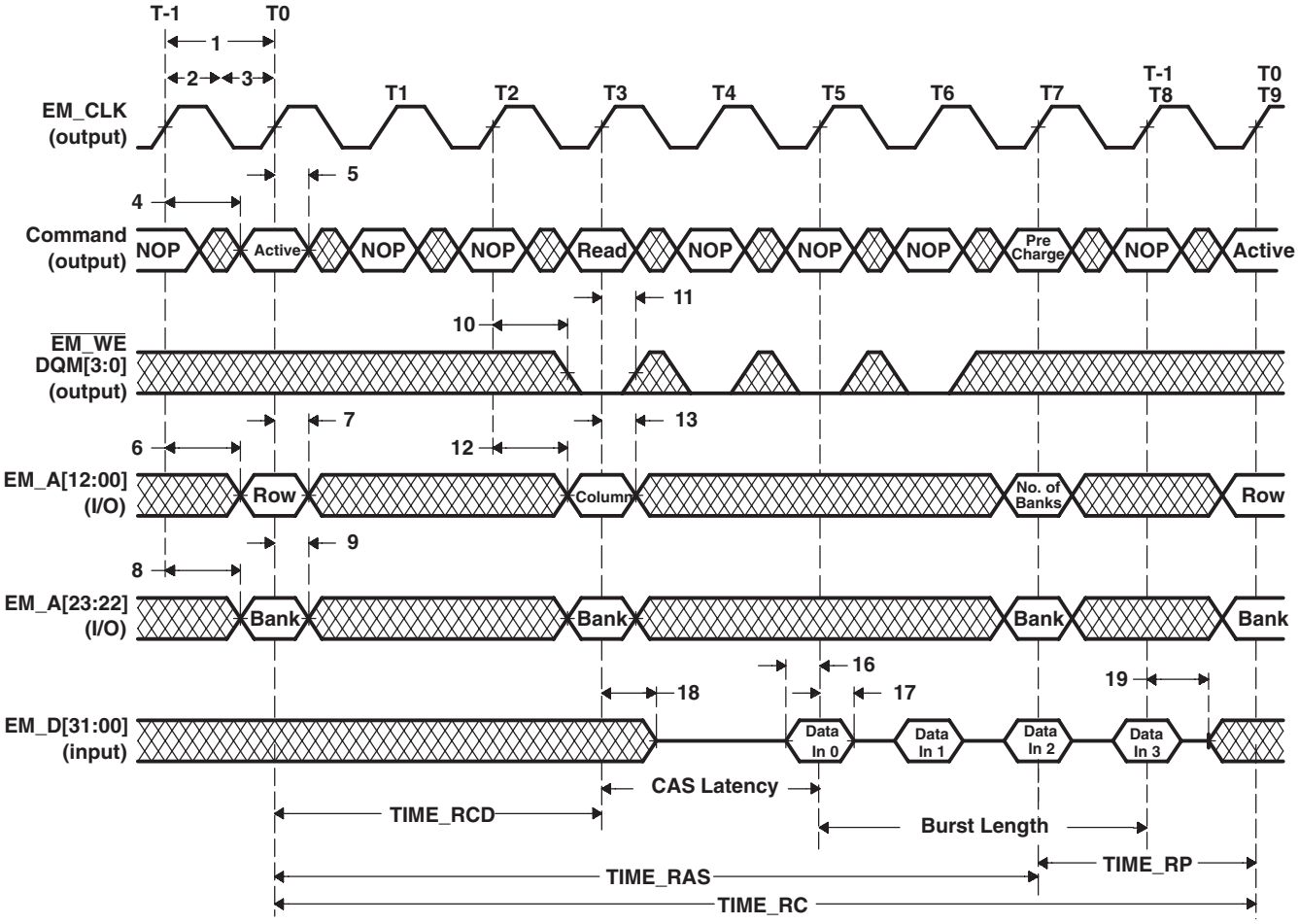


Figure 5-9 EMIF SDRAM Read



5.7.2 EMIF Asynchronous

Table 5-13 EMIF Asynchronous Timing

See Figure 5-10 through Figure 5-15					
No.	**Description**		**Min**	**Max**	**Unit**
	$f_{c(ASYNC\_CLK)}$	Frequency, EM_CLK		125	MHz
1	$t_{c(ASYNC\_CLK)}$	Cycle time, EM_CLK	8		ns
2	$t_{w(ASYNC\_CLK\_H)}$	Pulse duration, EM_CLK high	3.6		ns
3	$t_{w(ASYNC\_CLK\_L)}$	Pulse duration, EM_CLK low	3.6		ns
4	$t_{d(ADDR\_V)}$	Delay time, EM_CLK↑ to EM_A[23:00] valid	1.2	5.5	ns
5	$t_{d(ADDR\_I)}$	Delay time, EM_CLK↑ to EM_A[23:00] invalid	1.2	5.5	ns
6	$t_{d(DATA\_V)}$	Delay time, EM_CLK↑ to EM_D[31:00] valid	1.2	5.5	ns
7	$t_{d(DATA\_I)}$	Delay time, EM_CLK↑ to EM_D[31:00] invalid	1.2	5.5	ns
8	$t_{d(CS\_A)}$	Delay time, EM_CLK↑ to $\overline{EM\_CS[0,3,4,5]}$↓	1.2	5.5	ns
9	$t_{d(CS\_I)}$	Delay time, EM_CLK↑ to $\overline{EM\_CS[0,3,4,5]}$↑	1.2	5.5	ns
10	$t_{d(RW\_A)}$	Delay time, EM_CLK↑ to EM_R/$\overline{W}$↓	1.2	5.5	ns
11	$t_{d(RW\_I)}$	Delay time, EM_CLK↑ to EM_R/$\overline{W}$↑	1.2	5.5	ns
12	$t_{d(WE\_A)}$	Delay time, EM_CLK↑ to $\overline{EM\_WE}$↓	1.2	5.5	ns
13	$t_{d(WE\_I)}$	Delay time, EM_CLK↑ to $\overline{EM\_WE}$↑	1.2	5.5	ns
14	$t_{d(BYTE\_A)}$	Delay time, EM_CLK↑ to $\overline{EM\_WE\_DQM[3:0]}$↓	1.2	5.5	ns
15	$t_{d(BYTE\_I)}$	Delay time, EM_CLK↑ to $\overline{EM\_WE\_DQM[3:0]}$↑	1.2	5.5	ns
16	$t_{d(OE\_A)}$	Delay time, EM_CLK↑ to $\overline{EM\_OE}$↓	1	5.5	ns
17	$t_{d(OE\_I)}$	Delay time, EM_CLK↑ to $\overline{EM\_OE}$↑	1	5.5	ns
18	$t_{d(WAIT\_A)1}$	Setup, time, EM_WAIT to EM_CLK↑	4.5		ns
19	$t_{d(WAIT\_A)2}$	Hold time, EM_WAIT after EM_CLK↑	2.3		ns
20	$t_{d(DATA)1}$	Setup, time, EM_D[31:00] to EM_CLK↑	4.5		ns
21	$t_{d(DATA)2}$	Hold time, EM_D[31:00] after EM_CLK↑	2.3		ns
End of Table 5-13					

Each asynchronous chip select is provided with a control register, which allows individual adjustment of the write timing parameters (W_SU, W_STROBE, and W_HOLD), read timing parameters (R_SU, R_STROBE, and R_HOLD), and chip select delay timing (CS_DELAY). In addition, external wait states may be individually enabled for each asynchronous chip select with the polarity of the EM_WAIT input signal controlled through the register EMIF (ASYNC_WAIT_CONFIG). Byte enable control may also be enabled on asynchronous read events through this register set, allowing attachment to external static RAM devices requiring this feature. Note the timing differences introduced when evoking this byte-enable feature.

- $\overline{EM\_CS0}$, register EMIF (ASYNC_CONFIG_BANK_1)
- $\overline{EM\_CS3}$, register EMIF (ASYNC_CONFIG_BANK_2)
- $\overline{EM\_CS4}$, register EMIF (ASYNC_CONFIG_BANK_3)
- $\overline{EM\_CS5}$, register EMIF (ASYNC_CONFIG_BANK_4)

Figure 5-10 EMIF Asynchronous Write

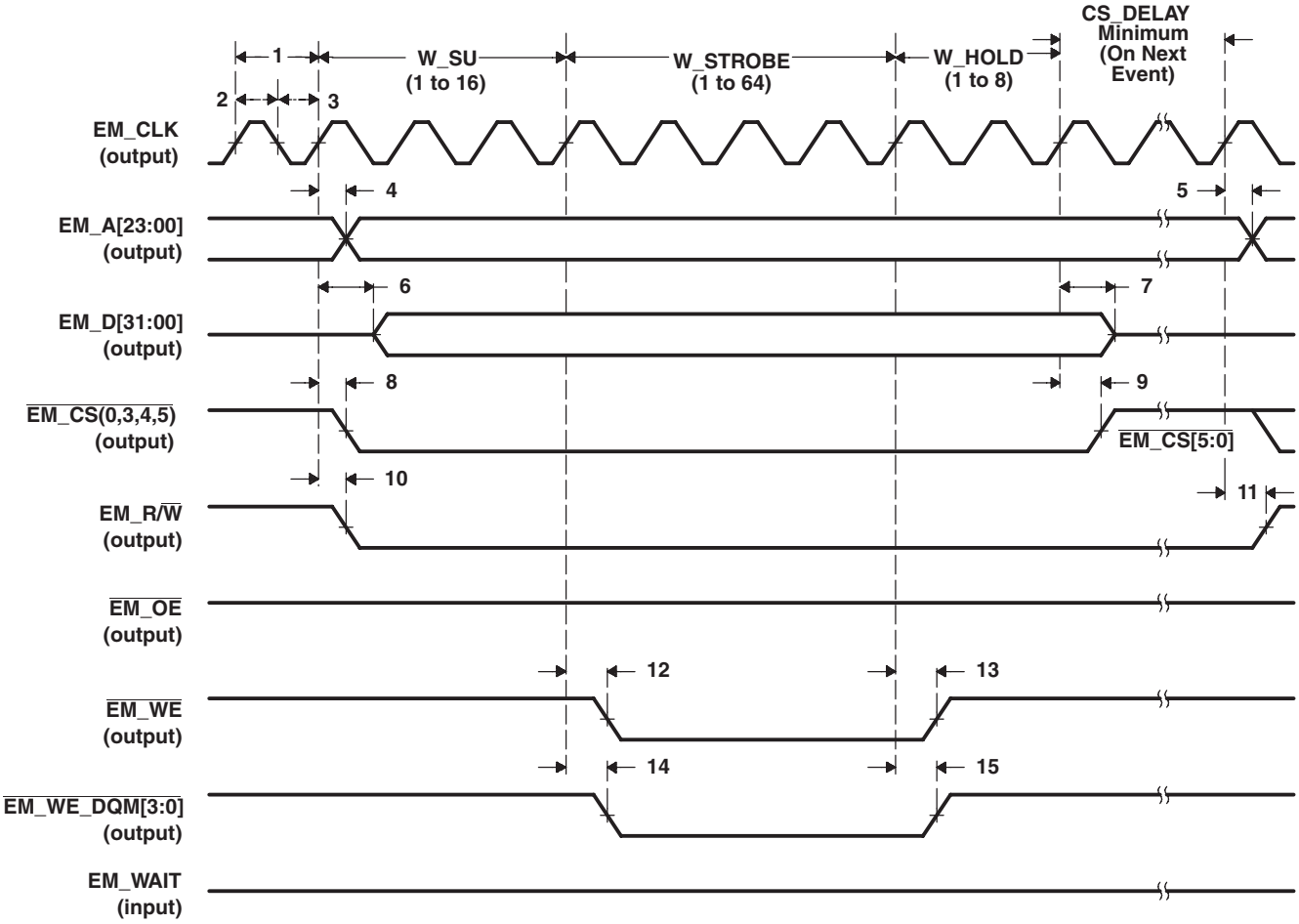


Figure 5-11 EMIF Asynchronous Read

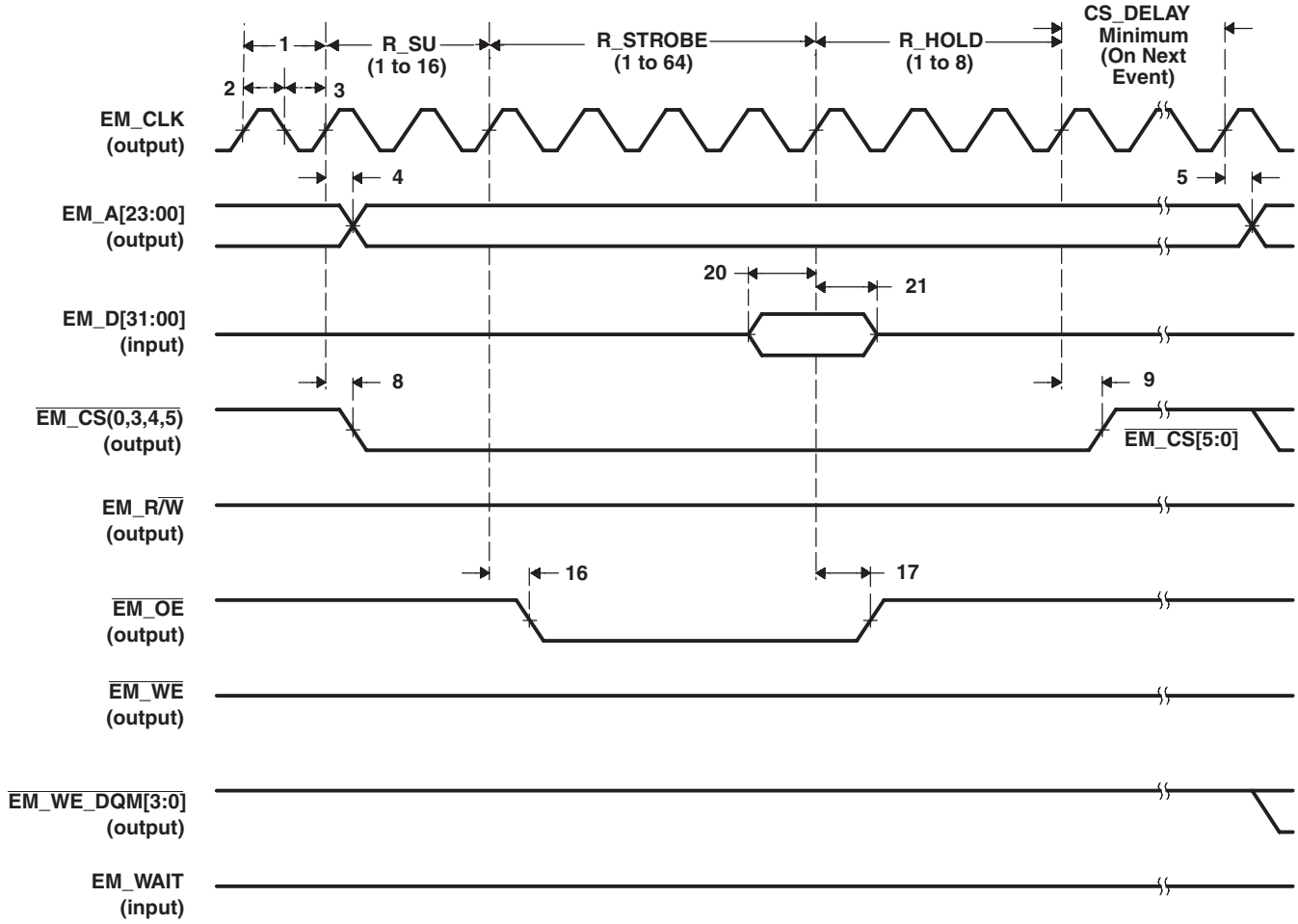


Figure 5-12 EMIF Asynchronous Write With Wait

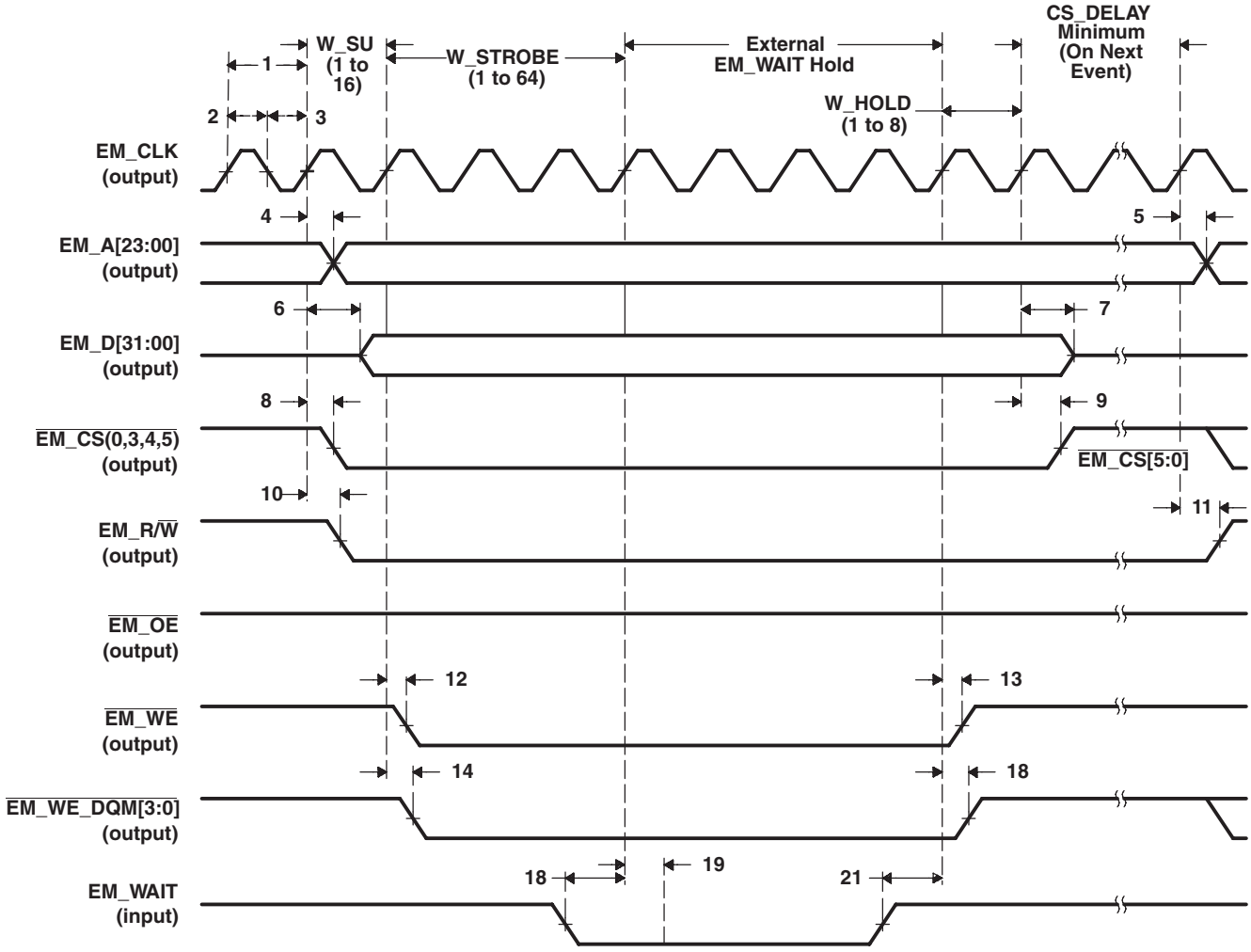


Figure 5-13 EMIF Asynchronous Read With Wait

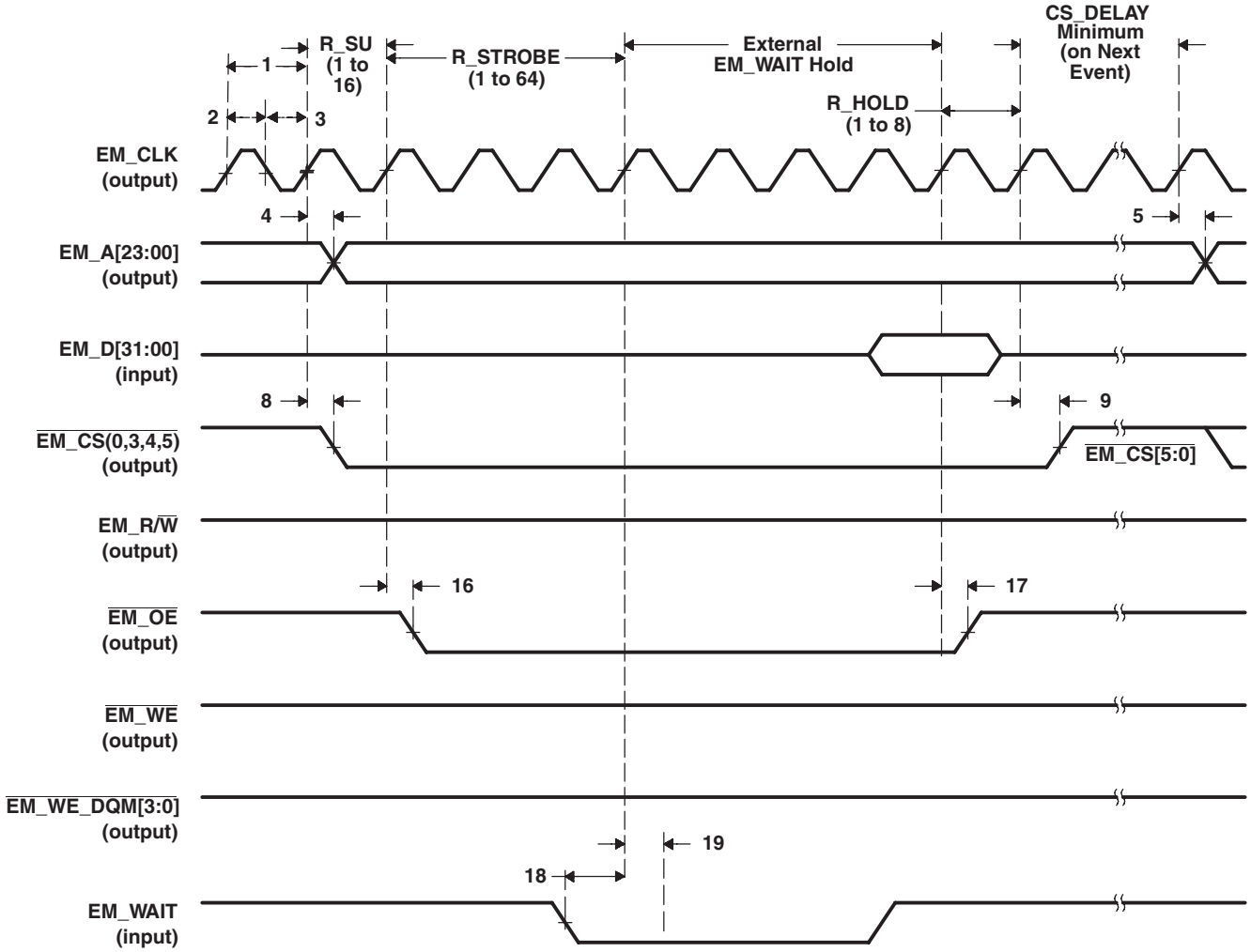


Figure 5-14 EMIF Asynchronous Write With Byte Enable

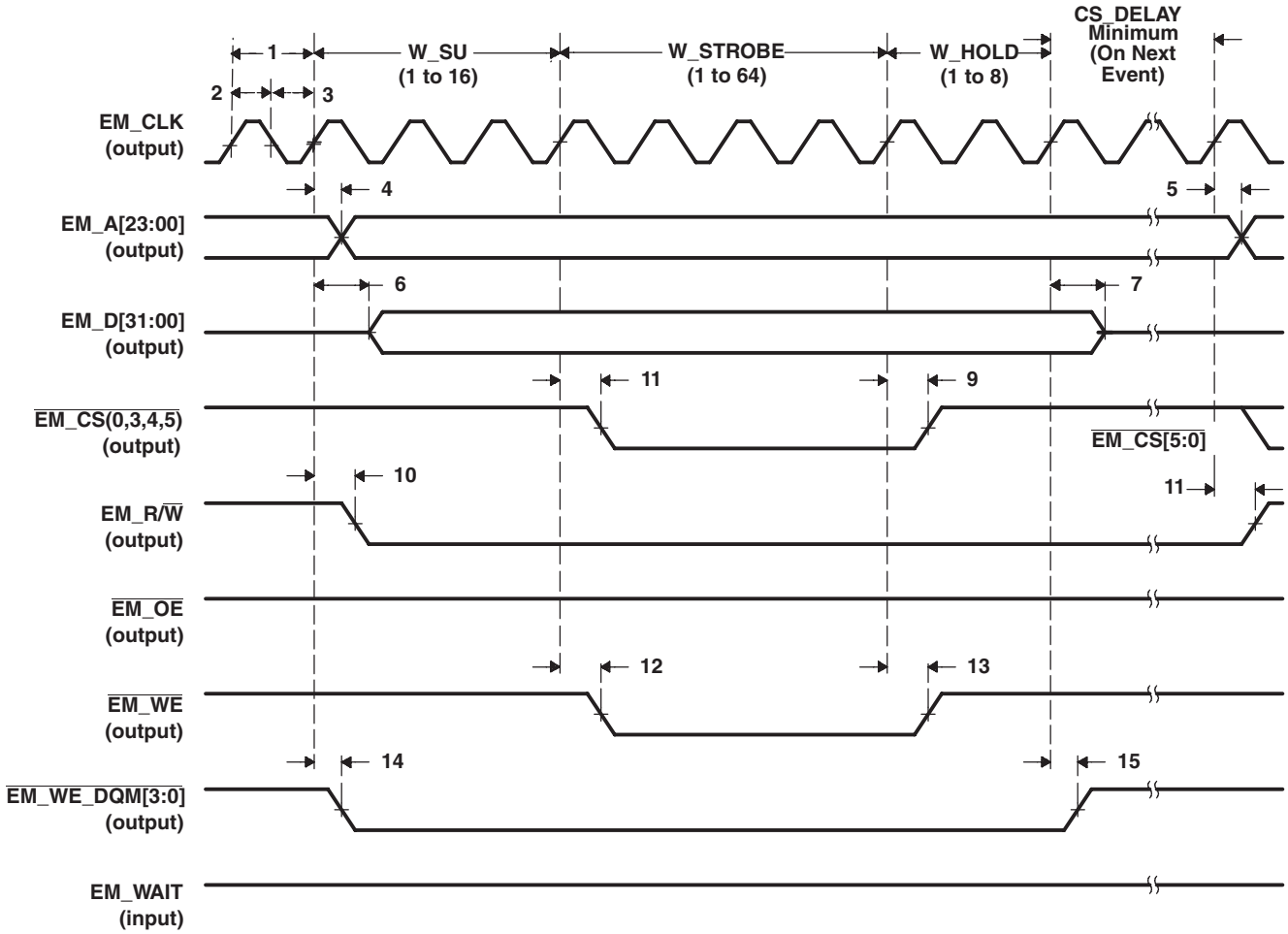
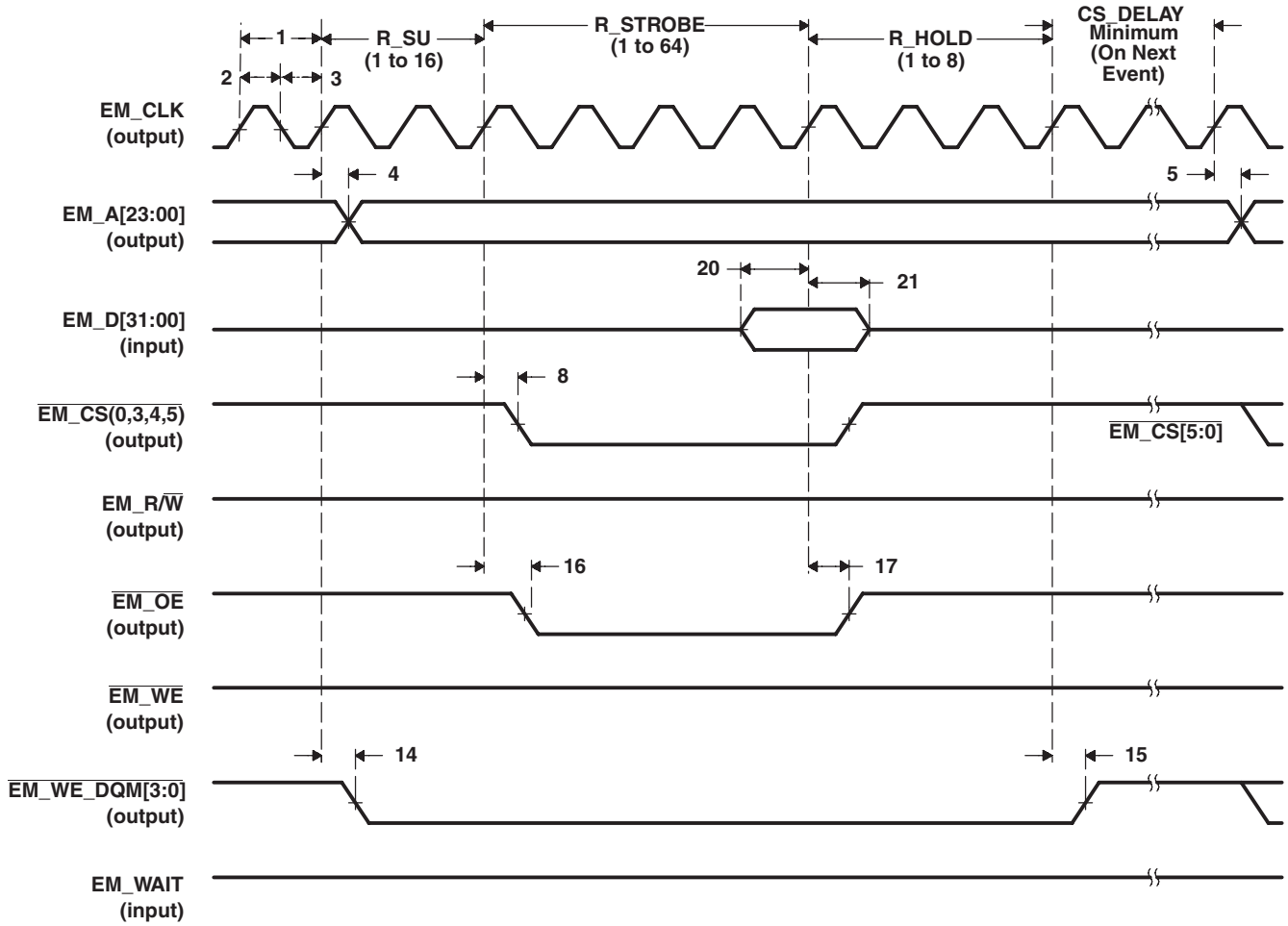


Figure 5-15 EMIF Asynchronous Read With Byte Enable



5.8 Ethernet Interface Timing

5.8.1 PHY

Table 5-14 Ethernet 10-MBit Transmit Timing

See Figure 5-16						
No.	**Description**		**Min**	**Typ**	**Max**	**Unit**
1	P0_TX_P, P0_TX_M	10-Mbit transmit voltage output high level (V_{T10H})	2.2	2.5	2.8	V
2		10-Mbit transmit voltage output mid level (V_{T10M})		0		V
3		10-Mbit transmit voltage output low level (V_{T10L})	–2.8	–2.5	–2.2	V
End of Table 5-14						

Figure 5-16 Ethernet 10-MBit Transmit

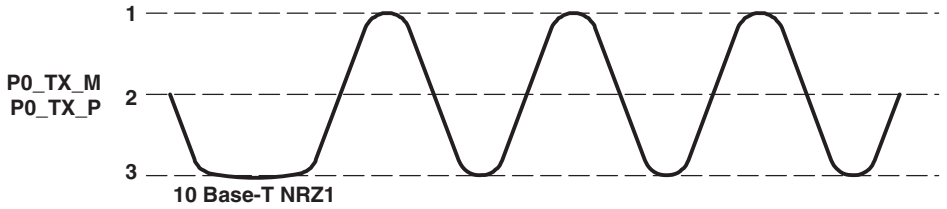


Table 5-15 Ethernet 100-MBit Transmit Timing

See Figure 5-17						
No.	**Description**		**Min**	**Typ**	**Max**	**Unit**
1	P0_TX_P, P0_TX_M	100-Mbit transmit voltage output high level (V_{T100H})	0.95	1	1.05	V
2		100-Mbit transmit voltage output mid level (V_{T100M})	–0.50	0	0.50	V
3		100-Mbit transmit voltage output low level (V_{T100L})	–1.05	–1	–0.95	V
4	$t_{r(T100\_m1)}$	Rise time, 100-Mbit transmit –1	3	4	5	ns
5	$t_{r(T100\_p1)}$	Rise time, 100-Mbit transmit 1	3	4	5	ns
6	$t_{f(T100\_p1)}$	Fall time, 100-Mbit transmit 1	3	4	5	ns
7	$t_{f(T100\_m1)}$	Fall time, 100-Mbit transmit –1	3	4	5	ns
8	$t_{d(T100\_JITTER)}$	Delay time, 100-Mbit transmit jitter			1.4	ns
End of Table 5-15						

Figure 5-17 Ethernet 100-Mbit Transmit

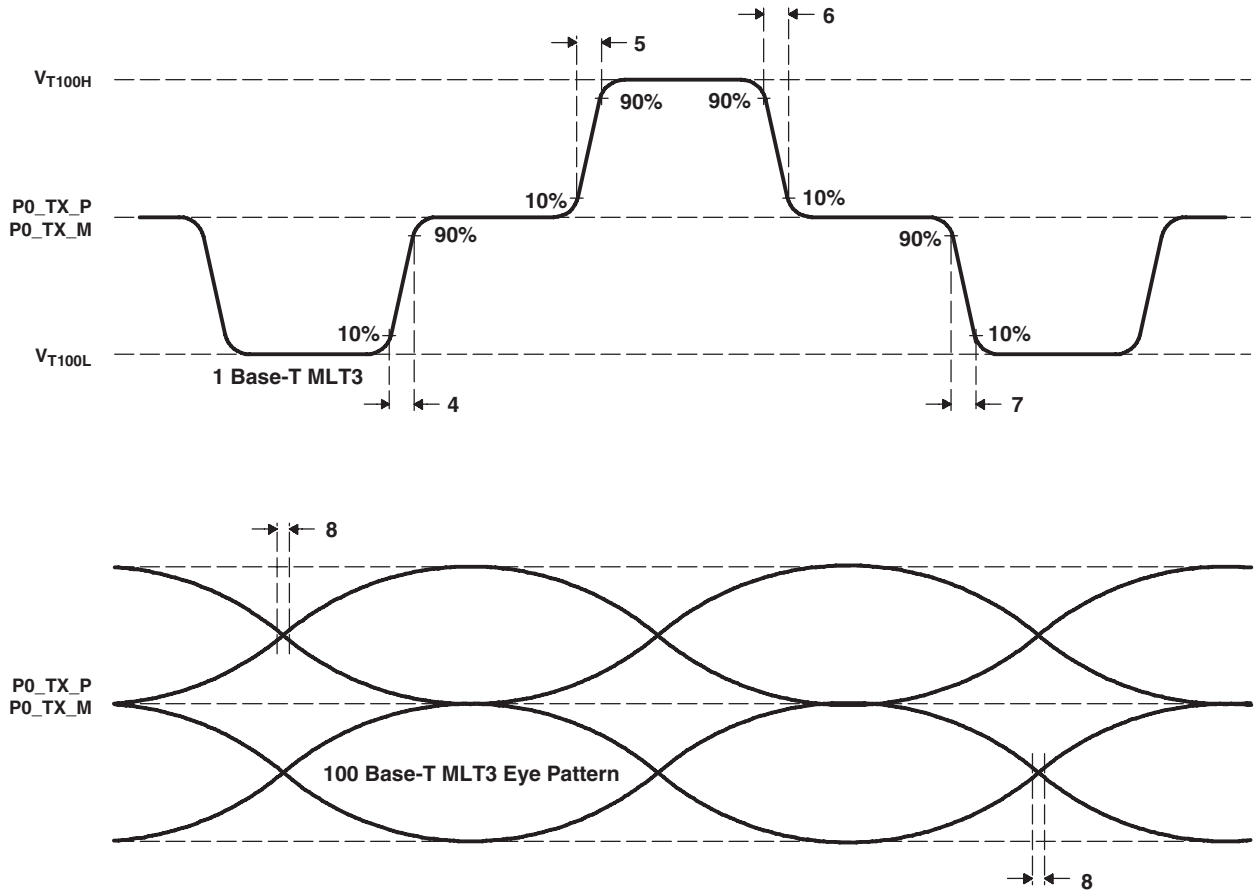


Table 5-16 Ethernet 10-Mbit Receive Timing

See Figure 5-18				
No.	**Description** [1]		**Typ**	**Unit**
1	P0_RX_P, P0_RX_M	10-Mbit receive peak-to-peak voltage input squelch (V_{R10ppS})	300	mV
2		10-Mbit receive peak-to-peak voltage input detect (V_{R10ppD})	585	mV
End of Table 5-16				

1 The equalizer function in the PHY compensates for phase and amplitude distortion in the physical channel (magnetics, connectors, and CAT 5 cable). The signal can be restored for any good quality CAT 5 cable length between 1 m and 150 m. If the DC content of the signal is such that the low-frequency component falls below the low-frequency pole of the isolation transformer, then the droop characteristics of the transformer becomes significant, and baseline wander (BLW) on the received signal results. To prevent corruption of the received data, the PHY corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD-defined killer packet with no bit errors.

Figure 5-18 Ethernet 10-Mbit Receive

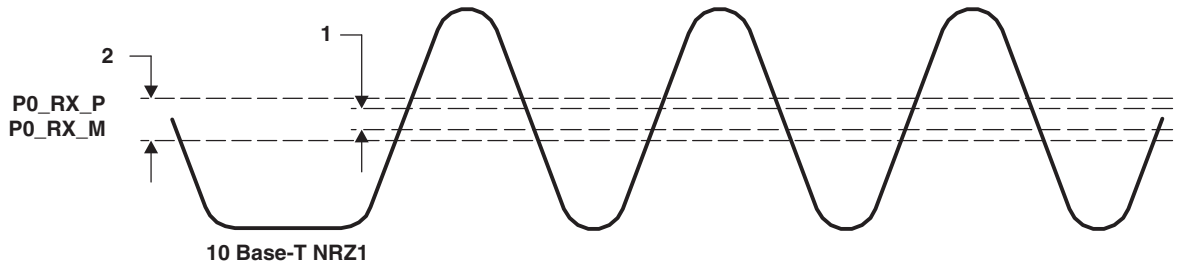
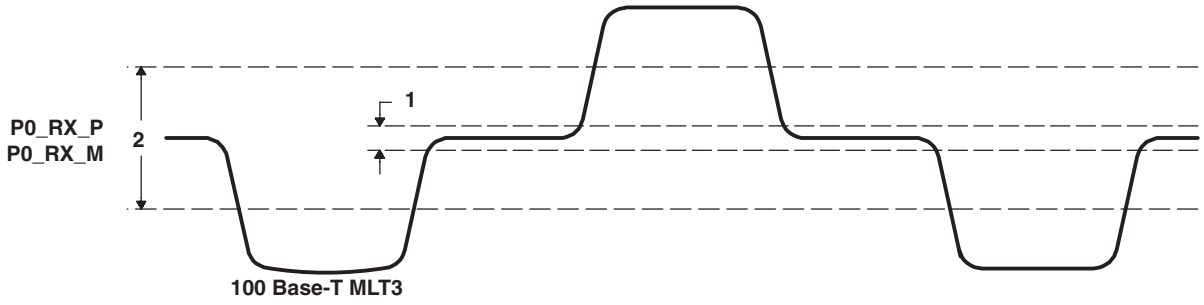


Table 5-17 Ethernet 100-Mbit Receive Timing

See Figure 5-19						
No.	**Description (1)**		**Min**	**Typ**	**Max**	**Unit**
1	P0_RX_P, P0_RX_M	100-Mbit receive peak-to-peak voltage input undetectable ($V_{R100ppOFF}$)	200			mV
2		100-Mbit receive peak-to-peak voltage input detectable ($V_{R100ppON}$)		300		mV
End of Table 5-17						

1 The equalizer function in the PHY compensates for phase and amplitude distortion in the physical channel (magnetics, connectors, and CAT 5 cable). The signal can be restored for any good quality CAT 5 cable length between 1 m and 150 m. If the DC content of the signal is such that the low-frequency component falls below the low-frequency pole of the isolation transformer, then the droop characteristics of the transformer becomes significant, and baseline wander (BLW) on the received signal results. To prevent corruption of the received data, the PHY corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD-defined killer packet with no bit errors.

Figure 5-19 Ethernet 100-Mbit Receive



5.8.2 MII

Table 5-18 Ethernet MII Transmit Port Timing Requirements

See Figure 5-20					
No.	**Description (1)**		**Min**	**Max**	**Unit**
1	$t_{c(MII\_TX\_CLK)1}$	Cycle time, MII_P0_TX_CLK (100 Base-T), f_c = 25 MHz	40		ns
2	$t_{w(MII\_TX\_CLK\_H)1}$	Pulse duration, MII_P0_TX_CLK high (100 Base-T)	16	24	ns
3	$t_{w(MII\_TX\_CLK\_L)1}$	Pulse duration, MII_P0_TX_CLK low (100 Base-T)	16	24	ns
4	$t_{c(MII\_TX\_CLK)2}$	Cycle time, MII_P0_TX_CLK(10 Base-T), f_c = 25 MHz	400		ns
5	$t_{w(MII\_TX\_CLK\_H)2}$	Pulse duration, MII_P0_TX_CLK high (10 Base-T) (2)	160	240	ns
6	$t_{w(MII\_TX\_CLK\_L)2}$	Pulse duration, MII_P0_TX_CLK low (10 Base-T) (2)	160	240	ns
End of Table 5-18					

1 MII_P0_CRS and MII_P0_COL are driven asynchronously by the PHY. MII_P0_TX_D[3:0] are driven by the reconciliation sublayer synchronous to MII_P0_TX_CLK. MII_P0_TX_ENBL is asserted and deasserted by the reconciliation sublayer synchronous to the rising edge of MII_P0_TX_CLK. The timing shown in Table 5-18 represents the internal PHY disabled mode; all other modes are not covered.

2 Specified by design

Table 5-19 Ethernet MII Transmit Port Operating Characteristics

See Figure 5-20					
No.	**Description (1)**		**Min**	**Max**	**Unit**
7	$t_{d(MII\_TX\_D\_V)}$	Delay time, MII_P0_TX_CLK↑ to MII_P0_TX_D[3:0] valid	0	25	ns
8	$t_{d(MII\_TX\_ENBL\_V)}$	Delay time, MII_P0_TX_CLK↑ to MII_P0_TX_ENBL valid (2)	0	25	ns
9	$t_{d(MII\_TX\_ENBL\_I)}$	Delay time, MII_P0_TX_CLK↑ to MII_P0_TX_ENBL invalid (2)	0	25	ns
End of Table 5-19					

1 MII_P0_CRS and MII_P0_COL are driven asynchronously by the PHY. MII_P0_TX_D[3:0] are driven by the reconciliation sublayer synchronous to MII_P0_TX_CLK. MII_P0_TX_ENBL is asserted and deasserted by the reconciliation sublayer synchronous to the rising edge of MII_P0_TX_CLK. The timing shown in Table 5-19 represents the internal PHY disabled mode; all other modes are not covered.

2 Specified by design

Figure 5-20 Ethernet MII Transmit Port

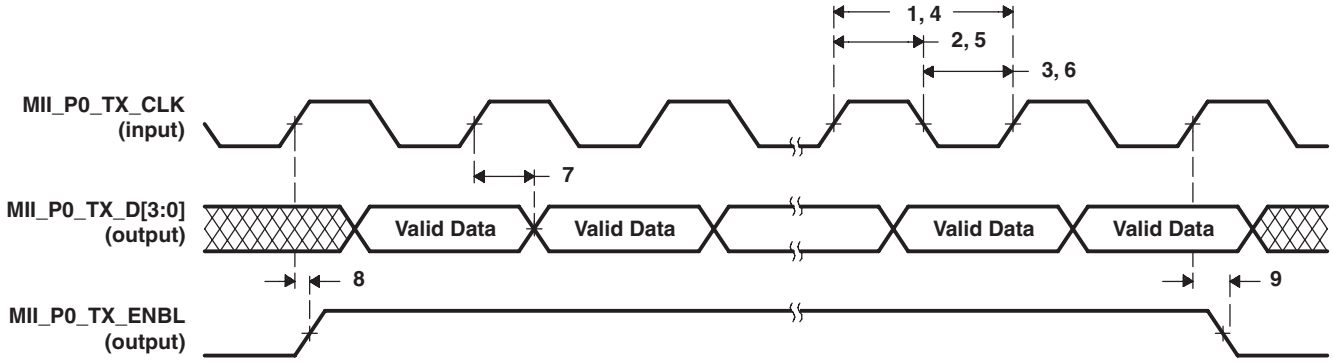


Table 5-20 Ethernet MII Receive Port Timing Requirements

See Figure 5-21

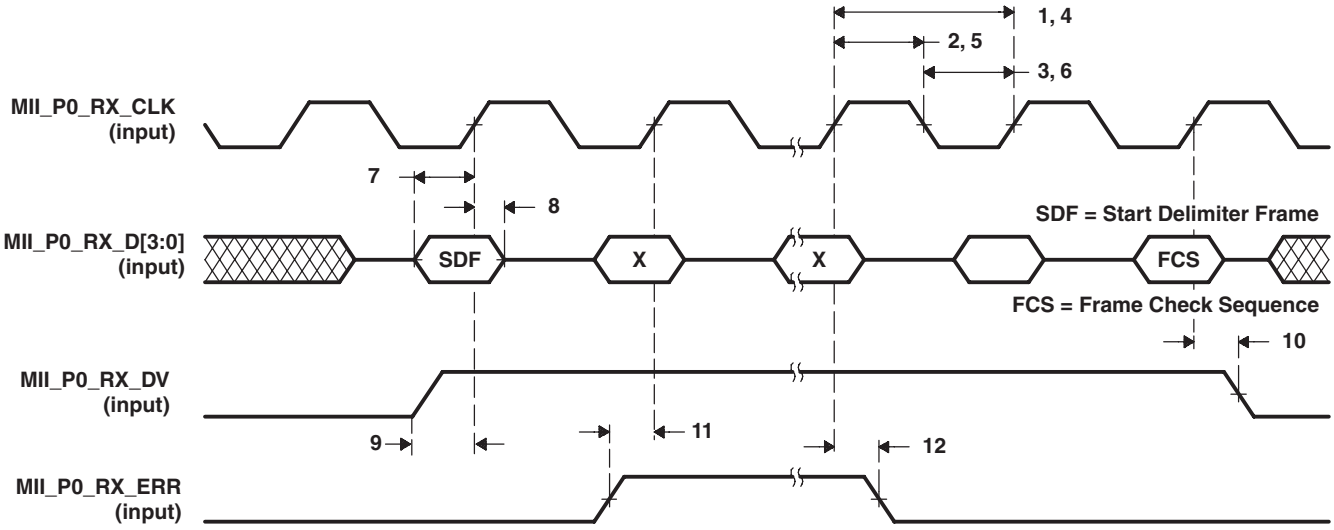
No.	Description (1)		Min	Max	Unit
1	$t_{c(MII\_RX\_CLK)1}$	Cycle time, MII_P0_RX_CLK (100 Base-T), f_c = 25 MHz	40		ns
2	$t_{w(MII\_RX\_CLK\_H)1}$	Pulse duration, MII_P0_RX_CLK high (100 Base-T)	16	24	ns
3	$t_{w(MII\_RX\_CLK\_L)1}$	Pulse duration, MII_P0_RX_CLK low (100 Base-T)	16	24	ns
4	$t_{c(MII\_RX\_CLK)2}$	Cycle time, MII_P0_RX_CLK(10 Base-T), f_c = 25 MHz	400		ns
5	$t_{w(MII\_RX\_CLK\_H)2}$	Pulse duration, MII_P0_RX_CLK high (10 Base-T) (2)	160	240	ns
6	$t_{w(MII\_RX\_CLK\_L)2}$	Pulse duration, MII_P0_RX_CLK low (10 Base-T) (2)	160	240	ns
7	$t_{su(MII\_RX\_D)}$	Setup time, MII_P0_RX_D[3:0] valid before MII_P0_RX_CLK↑	5		ns
8	$t_{h(MII\_RX\_D)}$	Hold time, MII_P0_RX_D[3:0] valid after MII_P0_RX_CLK↑	5		ns
9	$t_{su(MII\_RX\_DV)}$	Setup time, MII_P0_RX_D[3:0] valid high before MII_P0_RX_CLK↑	5		ns
10	$t_{h(MII\_RX\_DV)}$	Hold time, MII_P0_RX_D[3:0]valid high after MII_P0_RX_CLK↑	5		ns
11	$t_{su(MII\_RX\_ERR)}$	Setup time, MII_P0_RX_ERR valid before MII_P0_RX_CLK↑	5		ns
12	$t_{h(MII\_RX\_ERR)}$	Hold time, MII_P0_RX_ERR valid after MII_P0_RX_CLK↑	5		ns

End of Table 5-20

1 MII_P0_CRS and MII_P0_COL are driven asynchronously by the PHY. MII_P0_RX_D[3:0] are driven by the PHY on the falling edge of MII_P0_RX_CLK. MII_P0_RX_D[3:0] timing must be met during clock periods when MII_P0_RX_DV is asserted, respectively. MII_P0_RX_DV is asserted and deasserted by the PHY on the falling edge of MII_P0_RX_CLK. MII_P0_RX_ERR is driven by the PHY on the falling edge of MII_P0_RX_CLK. The timing shown in Table 5-20 represents the Internal PHY disabled mode; all other modes are not covered.

2 Specified by design

Figure 5-21 Ethernet MII Receive Port



5.8.3 MDIO

Table 5-21 Ethernet MDIO Transmit Operating Characteristics

See Figure 5-22						
No.	**Description [1]**		**Min**	**Typ**	**Max**	**Unit**
	$f_{clock(MDIO\_CLK)}$	Clock frequency, MII_MD_CLK			8	MHz
1	$t_{c(MDIO\_CLK)}$	Cycle time, MII_MD_CLK	125			ns
2	$t_{w(MDIO\_CLK\_H)}$	Pulse duration, MII_MD_CLK high [2]		62.5		ns
3	$t_{w(MDIO\_CLK\_L)}$	Pulse duration, MII_MD_CLK low [2]		62.5		ns
4	$t_{d(MDIO\_TX\_D)}$	Delay time, MII_MD_CLK↑ to MII_MD_IO valid [2]	0		150	ns
End of Table 5-21						

1 The MDIO may be configured in any one of the following modes:
– Internal TNETV1056 driver. The TNETV1056 may control up to 30 external MII devices in this mode.
– External driver. An external device may control the two internal TNETV1056 PHY devices.
The timing shown in Table 5-21 represents the internal TNETV1056 driver mode; all other modes are not covered.

2 Specified by design

Figure 5-22 Ethernet MDIO Transmit

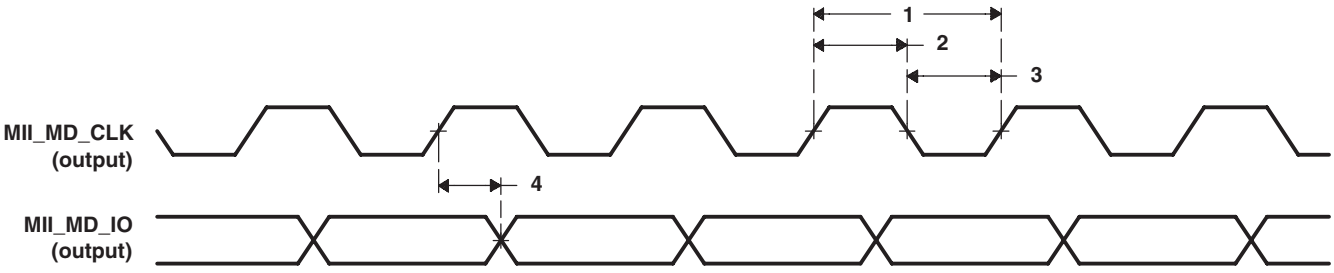


Table 5-22 Ethernet MDIO Receive Operating Characteristics

See Figure 5-23

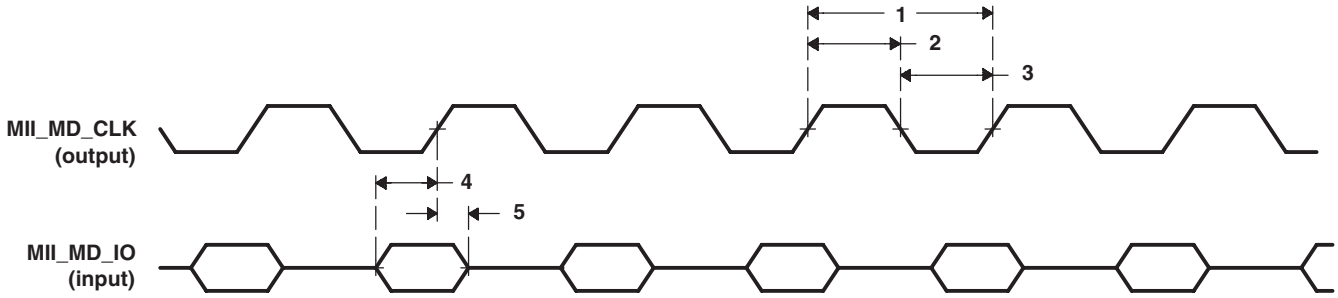
No.	Description (1)		Min	Typ	Max	Unit
	$f_{clockMDIO\_CLK)}$	Clock frequency, MII_MD_CLK			8	MHz
1	$t_{c(MDIO\_CLK)}$	Cycle time, MII_MD_CLK	125			ns
2	$t_{w(MDIO\_CLK\_H)}$	Pulse duration, MII_MD_CLK high (2)		62.5		ns
3	$t_{w(MDIO\_CLK\_L)}$	Pulse duration, MII_MD_CLK low (2)		62.5		ns
4	$t_{d(MDIO\_RX\_D)}$	Delay time, MII_MD_IO valid to MII_MD_CLK↑ (2)	10			ns
5	$t_{d(MDIO\_RX\_D)}$	Delay time, MII_MD_CLK↑ to MII_MD_IO valid (2)	5			ns

End of Table 5-22

1 The MDIO may be configured in any one of the following modes:
– Internal TNETV1056 driver. The TNETV1056 may control up to 30 external MII devices in this mode.
– External driver. An external device may control the two internal TNETV1056 PHY devices.
The timing shown in Table 5-22 represents the Internal TNETV1056 driver mode; all other modes are not covered.

2 Specified by design

Figure 5-23 Ethernet MDIO Receive



5.8.4 LED

Table 5-23 Ethernet LED Operating Characteristics

See Figure 5-24

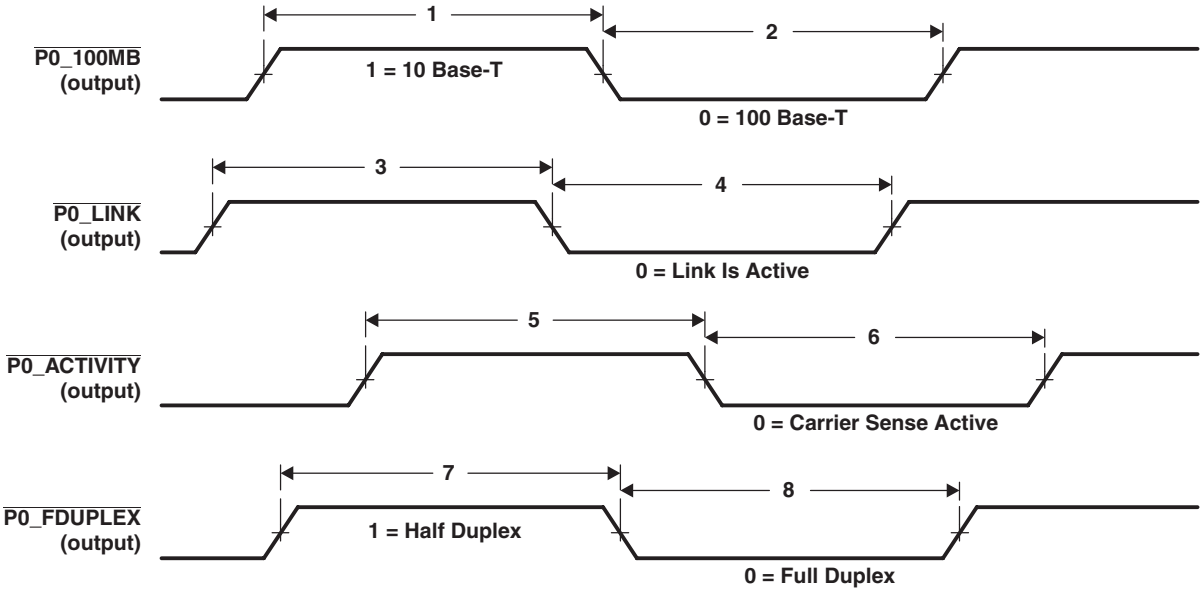
No.	Description (1)		Min	Max	Unit
1	$t_{w(LED\_100\_1)}$	Pulse duration, $\overline{P0\_100MB}$ high (2)	64		ms
2	$t_{w(LED\_100\_0)}$	Pulse duration, $\overline{P0_100MB}$low (2)	64		ms
3	$t_{w(LED\_LINK\_1)}$	Pulse duration, $\overline{P0\_LINK}$ high (2)	64		ms
4	$t_{w(LED\_LINK\_0)}$	Pulse duration, $\overline{P0\_LINK}$ low (2)	64		ms
5	$t_{w(LED\_ACTIVITY\_1)}$	Pulse duration, $\overline{P0\_ACTIVITY}$ high (2)	64		ms
6	$t_{w(LED\_ACTIVITY\_0)}$	Pulse duration, $\overline{P0\_ACTIVITY}$ low (2)	128		ms
7	$t_{w(LED\_DUPLEX\_1)}$	Pulse duration, $\overline{P0\_FDUPLEX}$ high (2)	64		ms
8	$t_{w(LED\_DUPLEX\_0)}$	Pulse duration, $\overline{P0\_FDUPLEX}$ low (2)	64		ms

End of Table 5-23

1 All LED output drivers are 8 mA, with an internal pullup.

2 Specified by design

Figure 5-24 Ethernet LED



5.9 Voice Codec

5.9.1 ADC Path Filter, Sampling Rate = 8 kHz

Table 5-24 ADC Channel Transfer (FIR) Response (Also Handset and Headset) (1)

Parameter	Test Conditions		Min	Max	Unit
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output, input signal is 0 dBm0	60 Hz		–34 (2)	dB
				–0.09	
		200 Hz		–1 (2)	
				–0.03	
		300 Hz		–0.06 (2)	
				–0.05	
		300 Hz to 2.4 kHz	–0.1	0.15	
		2.4 kHz to 3 kHz	–0.05	0.15	
		3 kHz to 3.4 kHz	–0.4	0.1	
		3.4 kHz to 3.6 kHz		–0.4	
		4 kHz		–26	
		4.5 kHz to 72 kHz		–52	
End of Table 5-24					

1 The filter gain for both outside of the bandpass is measured with respect to the gain at 1.02 kHz. The analog input test signal is –3 dB relative to 4-V_{pp} differential sine wave. The –3-dB passband is 0 to 3.6 kHz for an 8-kHz sampling rate and is 0 to 7.2 kHz for a sampling rate of 16 kHz. This passband scales linearly with the sampling rate.

2 With high-pass filter enabled, signals with frequencies below 300 Hz are attenuated.

Table 5-25 ADC Channel Transfer (IIR) Response (Also Handset and Headset) (1)

Parameter	Test Conditions		Min	Max	Unit
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output, input signal is 0 dBm0	60 Hz		–34 (2)	dB
				–0.15	
		200 Hz		–1 (2)	
				0.1	
		300 Hz		0.08 (2)	
				0.1	
		300 Hz to 2.4 kHz	–0.1	0.25	
		2.4 kHz to 3 kHz	–0.05	0.2	
		3 kHz to 3.4 kHz	–0.15	0.2	
		3.4 kHz to 3.6 kHz		0.15	
		4 kHz		–42	
		4.5 kHz to 72 kHz		–52	

1 The filter gain for both outside of the bandpass is measured with respect to the gain at 1.02 kHz. The analog input test signal is a –3-dB relative to 4-V_{pp} differential sine wave. The –3-dB passband is 0 to 3.6 kHz for an 8-kHz sampling rate and is 0 to 7.2 kHz for a sampling rate of 16 kHz. This passband scales linearly with the sampling rate.

2 With high-pass filter enabled, signals with frequencies below 300 Hz are attenuated.

5.9.2 ADC Dynamic Performance, Sampling Rate = 8 kHz

Table 5-26 ADC Signal-to-Noise With FIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal-to-noise ratio (SNR)	V_I = –3 dB	72	81		dB
	V_I = –9 dB	72	74		
End of Table 5-26					

1 The test condition is a 1020-Hz input differential signal with an 8-kHz conversion rate and BPF enabled. The input common mode is 1.35 V. The recommended maximum input is –3 dB relative to 4-V_{pp} differential to avoid SNDR droop.

Table 5-27 ADC Signal-to-Noise With IIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal-to-noise ratio (SNR)	V_I = –3 dB	72	81		dB
	V_I = –9 dB	72	74		
End of Table 5-27					

1 The test condition is a 1020-Hz input differential signal with an 8-kHz conversion rate. The input common mode is 1.35 V.

Table 5-28 ADC Signal-to-Distortion With FIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal-to-total harmonic distortion (THD)	V_I = –3 dB	72	84		dB
	V_I = –9 dB	72	95		
End of Table 5-28					

1 The test condition is a 1020-Hz input differential signal with an 8-kHz conversion rate. The input common mode is 1.35 V.

Table 5-29 ADC Signal-to-Distortion With IIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal-to-total harmonic distortion (THD)	V_I = –3 dB		84		dB
	V_I = –9 dB		93		
End of Table 5-29					

1 The test condition is a 1020-Hz input differential signal with an 8-kHz conversion rate. The input common mode is 1.35 V.

Table 5-30 ADC Signal-to-Distortion + Noise Using FIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal-to-total harmonic distortion + noise (THD + N)	V_I = –3 dB	72	81		dB
	V_I = –9 dB	72	74		
End of Table 5-30					

1 The test condition is a 1020-Hz input differential signal with an 8-kHz conversion rate. The input common mode is 1.35 V.

Table 5-31 ADC Signal-to-Distortion + Noise Using IIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal-to-total harmonic distortion + noise (THD + N)	V_I = –3 dB	70	80		dB
	V_I = –9 dB	70	74		
End of Table 5-31					

1 The test condition is a 1020-Hz input differential signal with an 8-kHz conversion rate. The input common mode is 1.35 V.

Table 5-32 Typical ADC Performance With PGA Gain Setting Using FIR (1)

PGA Gain Setting	SNR (dB)	THD (dB)	SINAD (dB)
9 dB	80	84	80
18 dB	80	84	80
24 dB	79	84	79
30 dB	79	84	79
36 dB	79	84	78

1 The test condition is a 1020-Hz input differential signal with an 8-kHz conversion rate. The input amplitude is such that output of PGA is a –3-dB level.

Table 5-33 ADC Channel Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{I(PP)}$	Differential-ended input level	PGA gain = 0 dB			4	V
V_{IO}	Input offset voltage			±5		mV
I_B	Input bias current			125		µA
	Common-mode voltage			1.35		V
	Dynamic range	V_I = –3 dB		81		dB
	Mute attenuation					
	Interchannel isolation			87		dB
E_G	Gain error	V_I = –3 dB at 1020 Hz		–0.45		dB
$E_{O(ADC)}$	ADC converter offset error			±15		mV
CMRR	Common-mode rejection ratio at INMx and INPx	V_I = 100 mV at 1020 Hz		50		dB
	Idle channel noise	V_{IN} = 0 V		30	70	μV_{rms}
R_j	Input resistance	TA = 25×C		10		kΩ
C_j	Input capacitance	TA = 25×C		2		pF
IIR	Channel delay			$5/f_s$		s
FIR	Channel delay			$17/f_s$		s
End of Table 5-33						

5.9.3 DAC Path Filter, Sampling Rate = 8 kHz

Table 5-34 DAC Channel Transfer (FIR) (1)

Parameter	Test Conditions		Min	Typ	Max	Unit
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output, input signal is 0 dBm0	0 Hz to 200 Hz			0.1	dB
		200 Hz to 300 Hz			–0.05	
		300 Hz to 2.4 kHz	–0.25		0.15	
		2.4 kHz to 3 kHz	–0.3		0.1	
		3 kHz to 3.4 kHz	–0.55		0.05	
		3.4 kHz to 3.6 kHz			–0.3	
		4 kHz			–28	
		4.5 kHz to 72 kHz			–70	
End of Table 5-34						

1 The test condition is a 1020-Hz input differential signal with an 8-kHz conversion rate. The input amplitude is such that output of PGA is a –3-dB level.

Table 5-35 DAC Channel Transfer (IIR) (1)

Parameter	Test Conditions		Min	Typ	Max	Unit
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output, input signal is 0 dBm0	0 Hz to 200 Hz			0.05	dB
		200 Hz to 300 Hz			0.05	
		300 Hz to 2.4 kHz	–0.1		0.1	
		2.4 kHz to 3 kHz	–0.2		0.1	
		3 kHz to 3.4 kHz	–0.25		0.05	
		3.4 kHz to 3.6 kHz			0	
		4 kHz			–34	
		4.5 kHz to 72 kHz			–70	
End of Table 5-35						

1 The filter gain outside of the bandpass is measured with respect to gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 4 Vpp. The –3-dB passband is 0 Hz to 3.6 kHz for an 8-kHz sample rate.

5.9.4 DAC Dynamic Performance

Table 5-36 Signal to Noise Using FIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal-to-noise ratio (SNR)	V_I = 0 dB		82		dB
	V_I = –9 dB		79		
End of Table 5-36					

1 The test condition is the digital equivalent of a 1020-Hz input signal with 8-kHz conversion rate. The test is measured at the low-pass filter in application schematic. The test is conducted in 16-bit mode.

Table 5-37 Signal to Noise Using IIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal-to-noise ratio (SNR)	V_I = 0 dB		71		dB
	V_I = –9 dB		70		
End of Table 5-37					

1 The test condition is the digital equivalent of a 1020-Hz input signal with 8-kHz conversion rate. The test is measured at the low-pass filter in application schematic. The test is conducted in 16-bit mode.

Table 5-38 Signal to Distortion Using FIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal to total harmonic distortion (THD)	V_I = –3 dB		83		dB
	V_I = –9 dB		84		
End of Table 5-38					

1 The test condition is the digital equivalent of a 1020-Hz input signal with 8-kHz conversion rate. The test is measured at the low-pass filter in application schematic. The test is conducted in 16-bit mode.

Table 5-39 Signal to Distortion Using IIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal to total harmonic distortion (THD)	V_I = –3 dB		83		dB
	V_I = –9 dB		84		
End of Table 5-39					

1 The test condition is the digital equivalent of a 1020-Hz input signal with 8-kHz conversion rate. The test is measured at the low-pass filter in application schematic. The test is conducted in 16-bit mode.

Table 5-40 Signal to Distortion + Noise Using FIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal to total harmonic distortion + noise (THD + N)	V_I = –3 dB		79		dB
	V_I = –9 dB		78		
End of Table 5-40					

1 The test condition is the digital equivalent of a 1020-Hz input signal with 8-kHz conversion rate. The test is measured at the low-pass filter in application schematic. The test is conducted in 16-bit mode.

Table 5-41 Signal to Distortion + Noise Using IIR Filter (1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Signal to total harmonic distortion + noise (THD + N)	V_I = –3 dB		71		dB
	V_I = –9 dB		70		
End of Table 5-41					

1 The test condition is the digital equivalent of a 1020-Hz input signal with 8-kHz conversion rate. The test is measured at the low-pass filter in application schematic. The test is conducted in 16-bit mode.

Table 5-42 DAC Channel Characteristics (1)

	Parameter	Test Conditions	Min	Typ	Max	Unit
	Dynamic range	V_I = 0 dB at 1020 Hz		82		dB
	Interchannel isolation			90		dB
E_G	Gain error, 0 dB	V_O = 0 dB at 1020 Hz		–0.3		dB
	Mute attenuation			90		dB
	Common-mode voltage			1.35		V
	Idle channel narrowband noise	0 to 4 kHz		40		μV_{rms}
V_{OO}	Output offset voltage at OUTP1_150 (differential)	DIN = all zeros		±8		mV
V_O	Analog output voltage (3.3 V)	OUTP1_150	0.25		2.35	V
IIR	Channel delay			$5/f_s$		s
FIR	Channel delay			$18/f_s$		s
End of Table 5-42						

1 The conversion rate is 8 kHz.

5.9.5 Speaker Interface

Table 5-43 Speaker Interface Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Speaker output power	V_{CC} = 3.3 V, fully differential, 8-Ω load (trace resistance from the output terminals to the speaker should be less than 0.05 Ω)		360		mW
Maximum output current	8-Ω load		0.3		A
End of Table 5-43					

5.9.6 Handset and Headset Interface

Table 5-44 Handset and Headset Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Speaker output power	V_{CC} = 3.3 V, fully differential, 150-Ω load		13		mW
Maximum output current	150-Ω load		13		mA
End of Table 5-44					

5.9.7 Line Interface

Table 5-45 Line Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Speaker output power	V_{CC} = 3.3 V, fully differential, 600-Ω load		3.3		mW
Maximum output current	600-Ω load		3.3		mA
End of Table 5-45					

5.9.8 BIAS Amplifier

Table 5-46 BIAS Amplifier Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Output voltage			1.35 or 2.35		V
Integrated noise	300 Hz to 13 kHz		20		µV
Offset voltage			10		mV
Current drive			5		mA
Unity-gain bandwidth			1		MHz
DC gain			90		dB
PSRR			70		dB
End of Table 5-46					

5.9.9 Power Supply

Table 5-47 Power-Supply Rejection (1)

Parameter		Test Conditions	Min	Typ	Max	Unit
AV_{DD}	Supply-voltage rejection ratio (PSRR), analog supply (f_j = 0 to f_s/2) at 1 kHz	Differential		75		dB
End of Table 5-47						

1 Power-supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV_{pp} signal applied to the appropriate supply.

5.10 McBSP Interface Timing

Table 5-48 McBSP Clock Operating Characteristics

See Figure 5-25

No.	Description (1)		Min	Typ	Max	Unit
	$f_{clock(CLKSRG\_DSP)}$	Clock frequency, CLKSRG, source ½ DSP_CLK (2)			62.5	MHz
1	$t_{c(CLKSRG\_DSP)}$	Cycle time, CLKSRG, source ½ DSP_CLK (2)	16			ns
2	$t_{w(CLKSRG\_DSP\_H)}$	Pulse duration, CLKSRG, source ½ DSP_CLK high (2)		8		ns
3	$t_{w(CLKSRG\_DSP\_L)}$	Pulse duration, CLKSRG, source ½ DSP_CLK low (2)		8		ns
	$f_{clock(CLKSRG\_CLKX)}$	Clock frequency, CLKSRG, source McBSP_CLK_TX (2)			8.192	MHz
6	$t_{c(CLKSRG\_CLKX)}$	Cycle time, CLKSRG, source McBSP_CLK_TX (2)	122			ns
7	$t_{w(CLKSRG\_CLKX\_H)}$	Pulse duration, CLKSRG, source McBSP_CLK_TX high (2)		61		ns
8	$t_{w(CLKSRG\_CLKX\_L)}$	Pulse duration, CLKSRG, source McBSP_CLK_TX low (2)		61		ns
	$f_{clock(CLKSRG\_CLKR)}$	Clock frequency, CLKSRG, source McBSP_CLK_RX (2)			8.192	MHz
11	$t_{c(CLKSRG\_CLKR)}$	Cycle time, CLKSRG, source McBSP_CLK_RX (2)	122			ns
12	$t_{w(CLKSRG\_CLKR\_H)}$	Pulse duration, CLKSRG, source McBSP_CLK_RX high (2)		61		ns
13	$t_{w(CLKSRG\_CLKR\_L)}$	Pulse duration, CLKSRG, source McBSP_CLK_RX low (2)		61		ns
	$f_{clock(CLKG\_O)}$	Clock frequency, CLKG, when used to drive McBSP_CLK_TX and/or McBSP_CLK_RX (2)			8.192	MHz
	$f_{clock(CLKG\_I)}$	Clock frequency, CLKG, when used for internal synchronization (2)			62.5	
16	$t_{c(CLKG)}$	Cycle time, CLKG (2)	1	X (3)	256	CLK_1 (4)
		External, driving McBSP_CLK_TX and/or McBSP_CLK_RX (2)	122			ns
		Internal use only, used for synchronization and may run faster (2)	16			
17	$t_{w(CLKG\_H)}$	Pulse duration, CLKG high — When X is even (2)	0.5	$(X/2)_t$	128	CLK_1
		Pulse duration, CLKG high — When X is odd and greater than 1 (2)		$(X/2)_t + 1$		
18	$t_{w(CLKG\_L)}$	Pulse duration, CLKG low (2)	0.5	$(X/2)_t$	128	CLK_1
19	$t_{w(FSG\_P)}$	Pulse duration, FSG pulse width (2)	1		256	CLK_2 (5)
20	$t_{w(FSG\_W)}$	Pulse duration, FSG period (2)	1		4096	CLK_2

End of Table 5-48

1 Programmable clock source: Either McBSP_CLK_TX, McBSP_CLK_RX, or ½ DSP_CLK may become the clock source, dependent on the state of the DSP_McBSP_EXT (SRGR) and DSP_McBSP_EXT (PCR) registers.

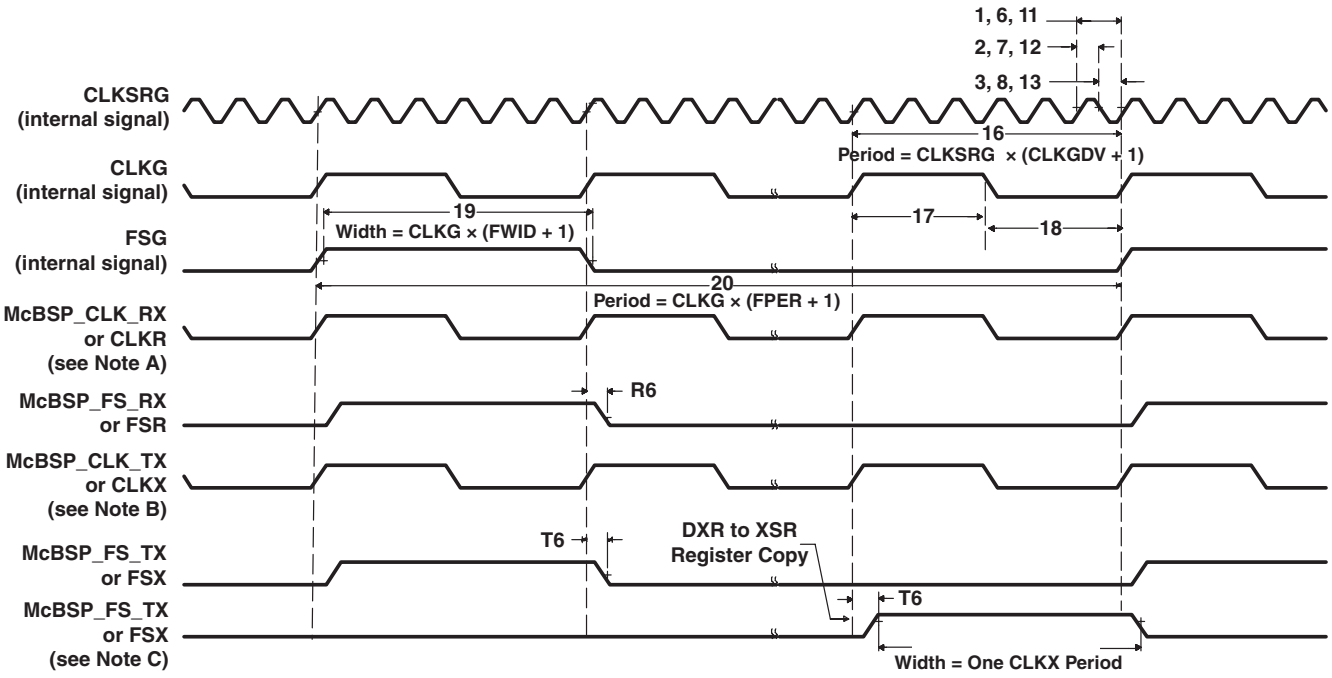
2 Specified by design

3 X: The total number of programmable clock-source periods defined in the DSP_McBSP_EXT (SRGR) register bits CLKGDV. The value X is (CLKDV + 1). In addition, the value $(X/2)_t$ is (½(CLKDV + 1)) truncated, except when CLKDV is 1.

4 CLK_1: Clock periods based on the programmable clock source

5 CLK_2: Clock periods based on CLKG

Figure 5-25 McBSP Clock



NOTES: A. When CLKR and FSR are not used as inputs, then they may be outputs generated by CLKG and FSG, with polarity defined by CLKRP and FSRP.
B. When CLKX and FSX are not used as inputs, then they may be outputs generated by CLKG and FSG, with polarity defined by CLKXP and FSXP.
C. Configured as an output, with FSGM = 0b, allowing an FSX on load of the serial transmit register.

Table 5-49 McBSP Transmit Timing

See Figure 5-26

No.		Description	CLKX	Min	Max	Unit
1	$t_{d(FSX\_OUT)}$	Delay time, McBSP_CLK_TX↑ to outbound McBSP_FS_TX↑ or ↓ (1)	Input	5	22	ns
			Output	1	6	
2	$t_{d(DX\_DXENA)}$	Delay time, McBSP_CLK_TX↑ to first McBSP_D_TX bit valid when DXENA is enabled (1) (2)	Input	2P + 5 (3)	2P + 22	ns
			Output	2P + 1	2P + 6	
3	$t_{d(DX\_V)}$	Delay time, McBSP_CLK_TX↑ to next McBSP_D_TX bit valid (1)	Input	5	22	ns
			Output	1	6	
4	$t_{d(DX\_I)}$	Delay time, McBSP_CLK_TX active to McBSP_D_TX high impedance (Z) after last bit (1)	Input	5	22	ns
			Output	1	6	
5	$t_{su(FSX\_IN)}$	Setup time, inbound McBSP_FS_TX high before McBSP_CLK_TX↓ (1)	Input	5		ns
			Output	22		
6	$t_{h(FSX\_IN)}$	Hold time, inbound McBSP_FS_TX high after McBSP_CLK_TX↓ (1)	Input	5		ns
			Output	10		

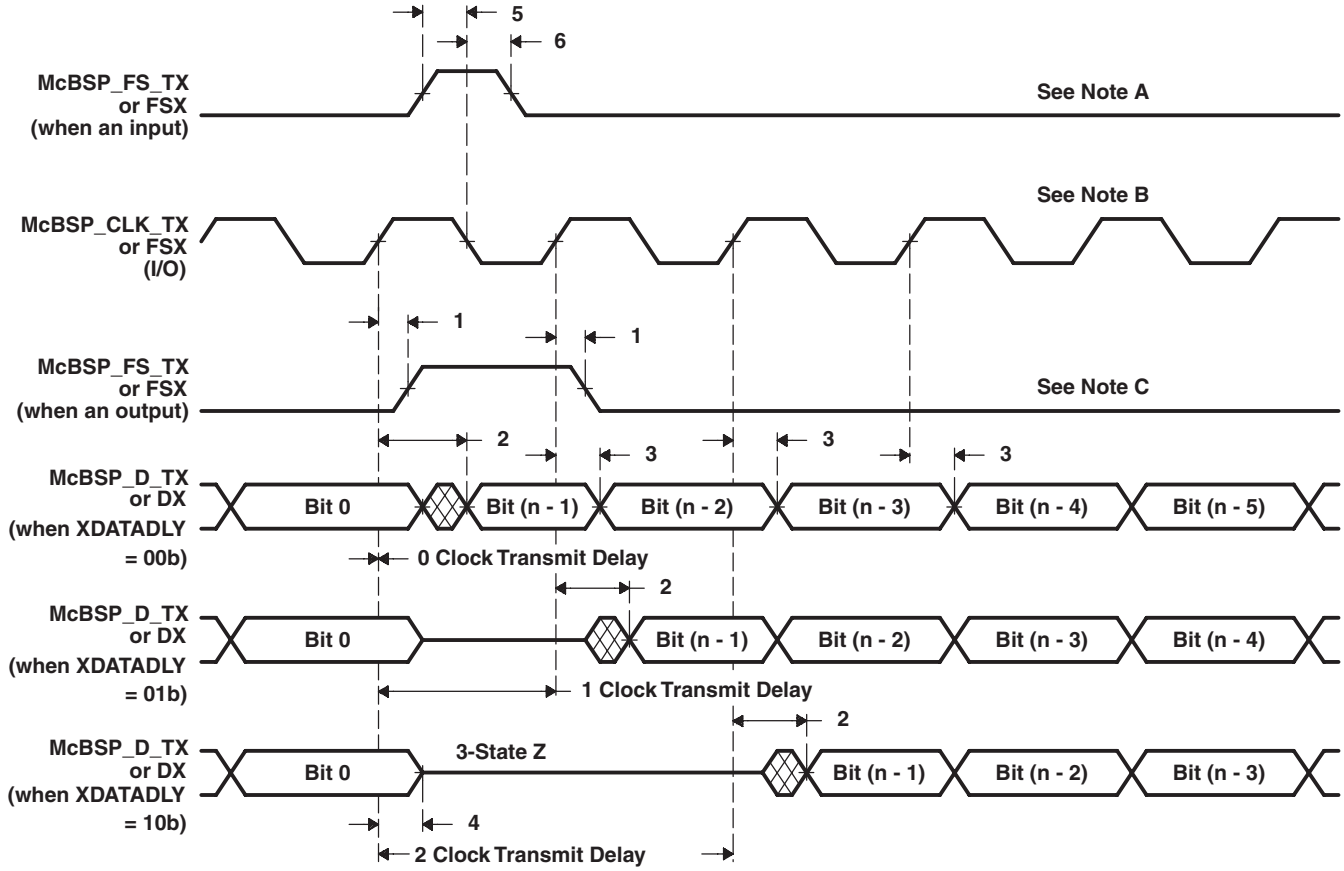
End of Table 5-49

1 Specified by design

2 When enabled, the DXENA bit in the DSP_McBSP_EXT (SPCR) register provides a two-clock-period (P) delay before the first data bit exits on McBSP_D_TX. Subsequent bits exit without the delay.

3 P = ½ DSP_CLK period

Figure 5-26 McBSP Transmit



NOTES: A. McBSP_FS_TX polarity may be inverted with the FSXP register bit.
B. McBSP_CLK_TX polarity may be inverted with the CLKXP register bit. All timing references are also inverted.
C. McBSP_FS_TX polarity may be inverted with the FSXP register bit.

Table 5-50 McBSP Receive Timing

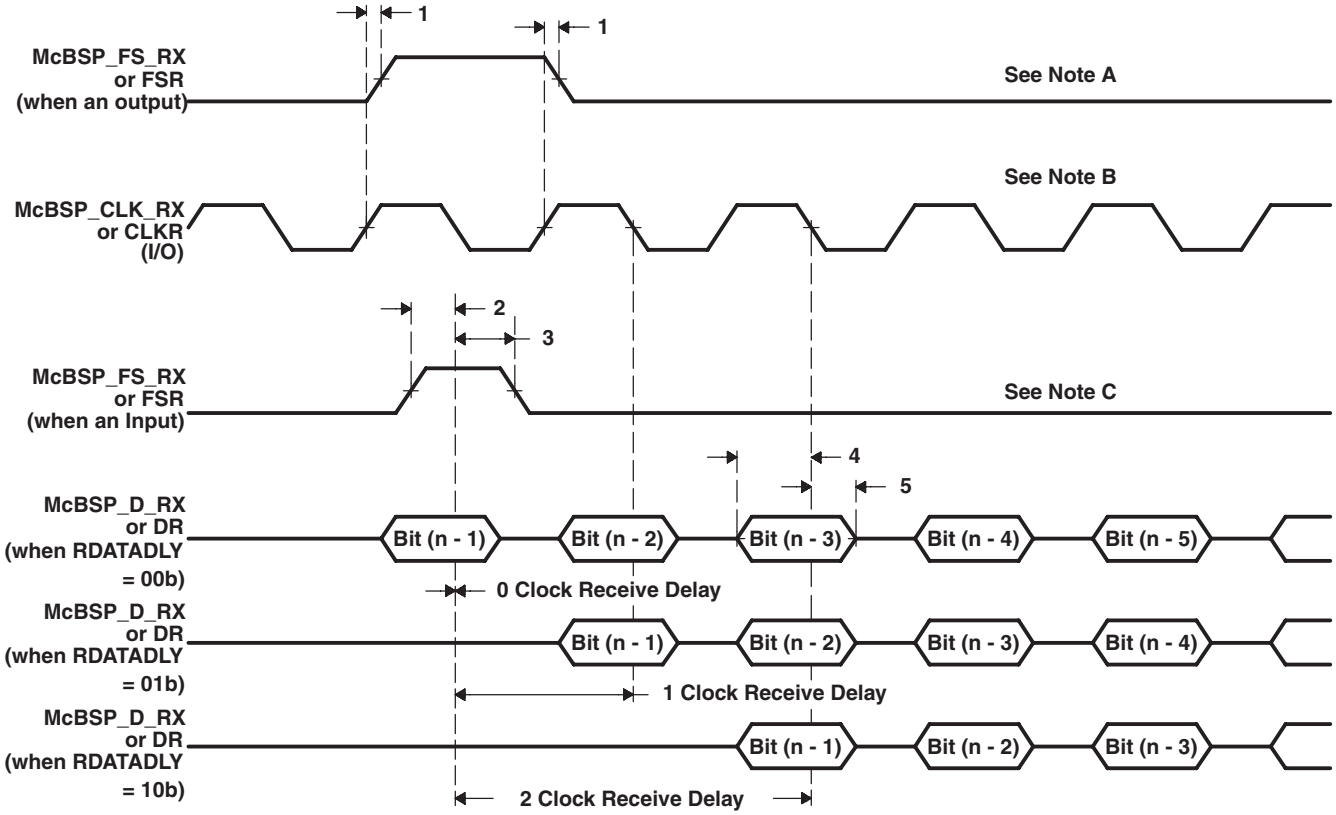
See Figure 5-27

No.		Description	CLKX	Min	Max	Unit
1	$t_{d(FSR\_OUT)}$	Delay time, McBSP_CLK_RX↑ to McBSP_FS_RX↑/↓ (1)	Input	5	22	ns
			Output	1	6	
2	$t_{su(FSR\_IN)}$	Setup time, inbound McBSP_FS_RX high before McBSP_CLK_RX↓ (1)	Input	5		ns
			Output	22		
3	$t_{h(FSR\_IN)}$	Hold time, inbound McBSP_FS_RX high after McBSP_CLK_RX↓ (1)	Input	5		ns
			Output	10		
4	$t_{su(DR)}$	Setup time, inbound McBSP_D_RX valid before McBSP_CLK_RX↓ (1)	Input	5		ns
			Output	22		
5	$t_{h(DR)}$	Hold time, inbound McBSP_D_RX valid after McBSP_CLK_RX↓ (1)	Input	5		ns
			Output	10		

End of Table 5-50

1 Specified by design

Figure 5-27 McBSP Receive



NOTES: A. McBSP_FS_RX polarity may be inverted with the FSRP register bit.
B. McBSP_CLK_RX polarity may be inverted with the CLKRP register bit. All timing references are also inverted.
C. McBSP_FS_RX polarity may be inverted with the FSRP register bit.

5.10.1 SPI Mode

Table 5-51 McBSP SPI Mode Master Timing

See Figure 5-28					
No.	**Description [1]**		**Min**	**Max**	**Unit**
	$f_{clock(SIP\_M\_CLKG)}$	Clock frequency, CLKG [2] [3]		8.192	MHz
1	$t_{c(SPI\_M\_CLKG)}$	Cycle time, CLKG [3]	122		ns
			2		CLK_1 [4]
2†	$t_{d(SPI\_M\_FSX\_A)}$	Delay time, CLKG↑ to McBSP_FS_TX↓ [3]	1	6	ns
3	$t_{d(SPI\_M\_FSX\_I)}$	Delay time, CLKG↑ to McBSP_FS_TX↑ [3]	1	6	ns
4	$t_{d(SPI\_M\_DX\_D)}$	Delay time, CLKG↓ to McBSP_D_TX valid driven [3]	1	6	ns
5	$t_{d(SPI\_M\_DX\_V)}$	Delay time, McBSP_CLK_TX↓ to McBSP_D_TX valid [3]	1	6	ns
6	$t_{d(SPI\_M\_DX\_I)}$	Delay time, McBSP_CLK_TX↓ to McBSP_D_TX invalid [3]	1	6	ns
7	$t_{su(SPI\_M\_DR)}$	Setup time, McBSP_D_RX valid before McBSP_CLK_TX↑ [3]	22		ns
8	$t_{h(SPI\_M\_DR)}$	Hold time, McBSP_D_RX valid after McBSP_CLK_TX↑ [3]	10		ns
9	$t_{w(SPI\_M\_FSX\_2)}$	Pulse duration, McBSP_FS_TX high [3]	2		CLK_2 [5]
End of Table 5-51					

1 SPI mode master: The McBSP is run in clock stop mode, with the McBSP providing clock timing through the internal generator (CLKG). The signals McBSP_CLK_TX, McBSP_FS_TX, and McBSP_D_TX are all outputs. The signal McBSP_D_RX is an input. The signals McBSP_CLK_RX and McBSP_FS_RX are not used, with McBSP_CLK_RX driven internally by McBSP_CLK_FX through an automatic connection.

2 The master clock polarity and delay are programmable, with the outcome shown in Figure 5-28.

3 Specified by design

4 CLK_1: Clock periods based on ½ DSP_CLK

5 CLK_2: Clock periods based on CLKG

Figure 5-28 McBSP SPI Mode Master

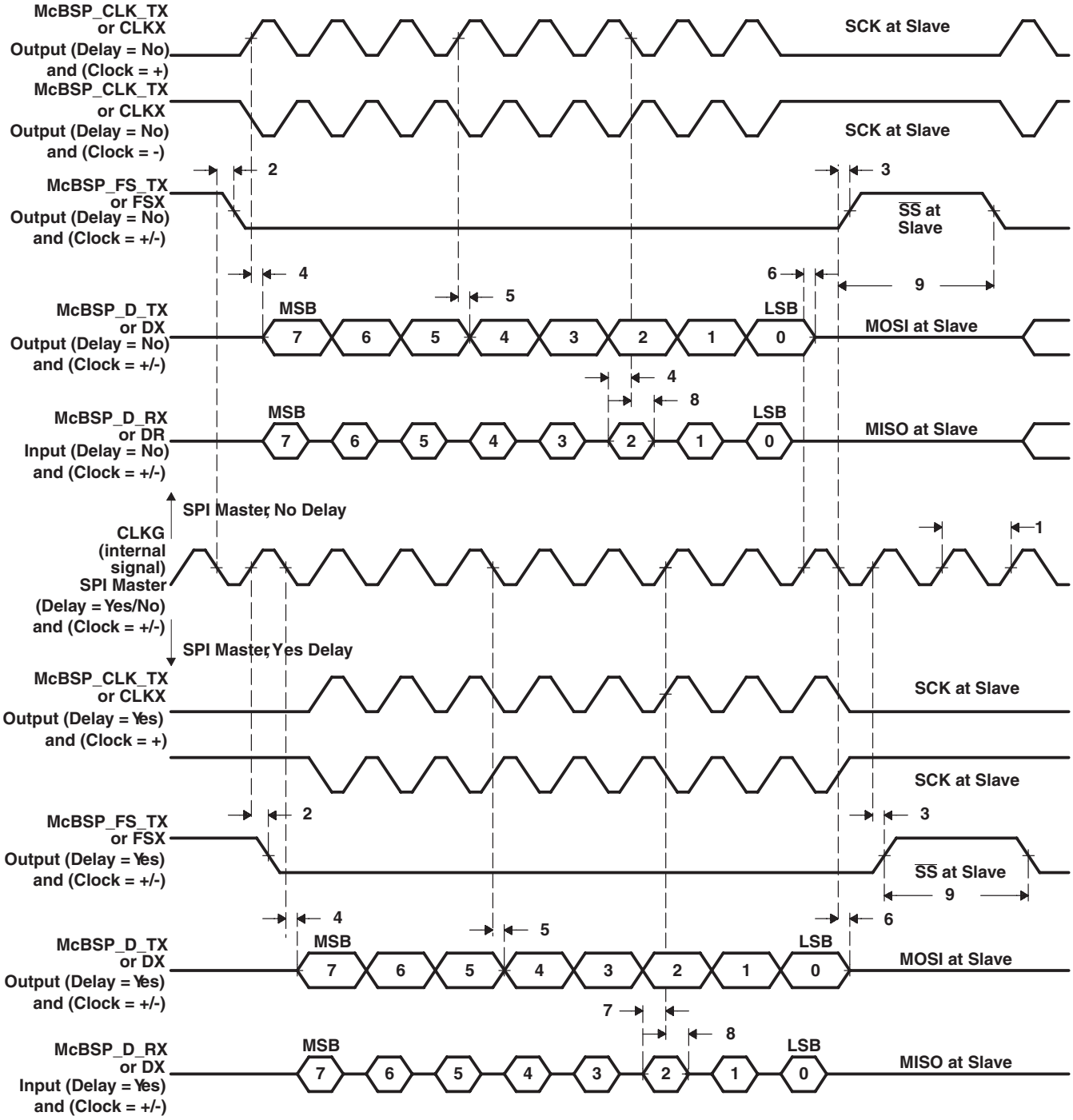


Table 5-52 McBSP SPI Mode Slave Timing

See Figure 5-29					
No.	**Description (1)**		**Min**	**Max**	**Unit**
	$f_{clock(SPI\_S\_CLKX)}$	Clock frequency, McBSP_CLK_TX, from master (2) (3)		3.90625	MHz
1	$t_{c(SPI\_S\_CLKX)}$	Cycle time, McBSP_CLK_TX, from master (3)	256		ns
1	$t_{c(SPI\_S\_CLKG)}$	Cycle time, CLKG, inside slave (3)	16		CLK_1 (4)
2	$t_{h(SPI\_S\_CLKX\_A)}$	Hold time, McBSP_FS_TX low before first McBSP_CLK_TX transition↑ (3) (5)	20		ns
3	$t_{d(SPI\_S\_DX\_A)}$	Delay time, McBSP_FS_TX↓ to McBSP_D_TX valid driven (3)	3P + 5 (6)	5P + 22	ns
4	$t_{d(SPI\_S\_DX\_V)}$	Delay time, McBSP_CLK_TX↑ to McBSP_D_TX valid (3)	3P + 5	3P + 22	ns
5	$t_{d(SPI\_S\_DX\_I)}$	Delay time, McBSP_CLK_TX↓ to McBSP_D_TX invalid released (3)	3P + 5	3P + 22	ns
6	$t_{su(SPI\_S\_DR)}$	Setup time, McBSP_D_RX valid before McBSP_CLK_TX↓ (3)	5		ns
7	$t_{h(SPI\_S\_DR)}$	Hold time, McBSP_D_RX valid after McBSP_CLK_TX↓ (3)	5		ns
8	$t_{w(SPI\_S\_FSX\_2)}$	Pulse duration, McBSP_FS_TX high, minimum idle duration (3)	2		CLK_2 (7)
End of Table 5-52					

1 SPI mode slave: The McBSP is run in clock stop mode with the external device performing all master functions. The signal McBSP_D_TX is an output. The signals McBSP_CLK_TX, McBSP_FS_TX, and McBSP_D_RX are all inputs. The signals McBSP_CLK_RX and McBSP_FS_RX are not used, with McBSP_CLK_RX driven internally by McBSP_CLK_FX through an automatic connection. Even though the external master device provides the clock through McBSP_CLK_TX, the internal clock generator must be activated and programmed to divide-by-two of the ½ DSP_CLK to provide proper synchronization.

2 Delay: In slave mode, the delay feature has no meaning and should not be programmed.

3 Specified by design

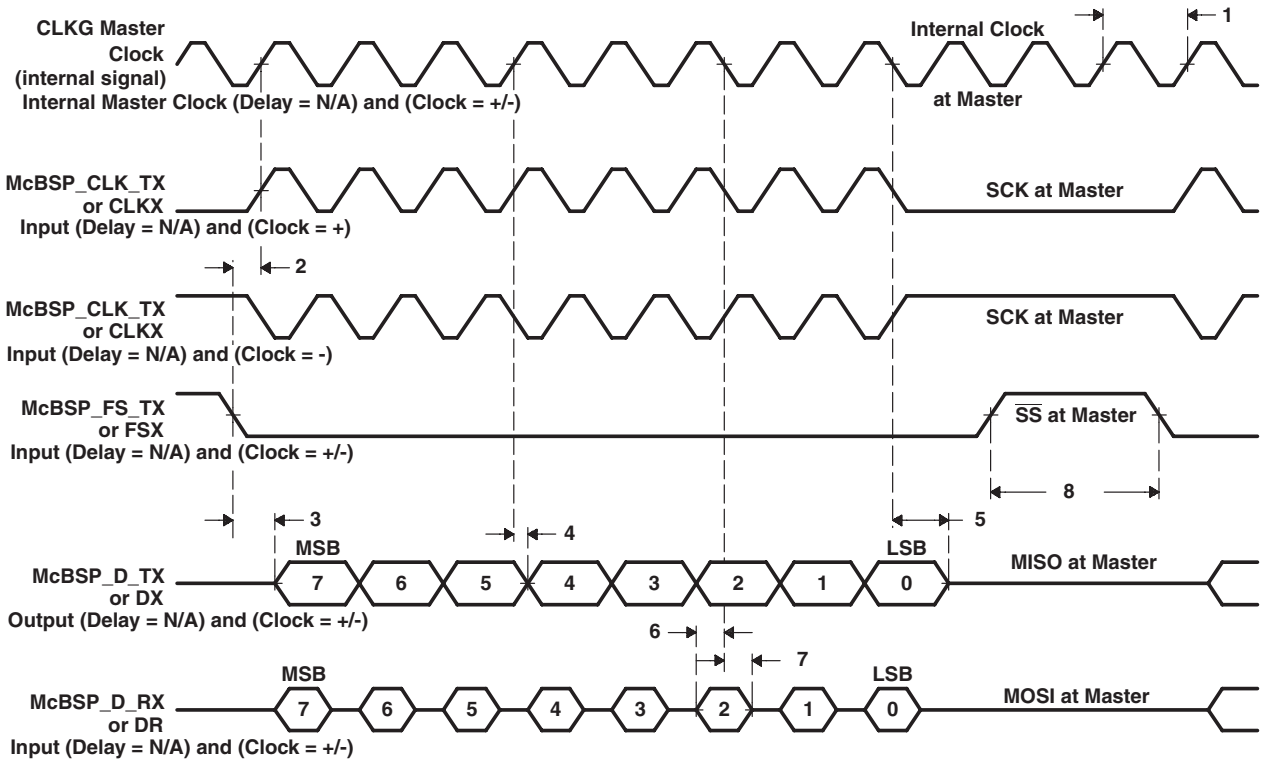
4 CLK_1: Clock periods based on ½ DSP_CLK

5 Clock polarity: The clock polarity is programmable, with the outcome shown in Figure 5-29.

6 P = clock period

7 CLK_2: Clock periods based on CLKG

Figure 5-29 McBSP SPI Mode Slave



5.11 Telephony Interface Timing

5.11.1 PCM

Table 5-53 Telephony Interface PCM Timing

See Figure 5-30

No.	Description		Min	Typ	Max	Unit
	$f_{clock(TELE\_CLK\_I)}$	Clock frequency, TELE_CLK_I (programmable clock source) (1) (2)			50	MHz
1	$t_{c(TELE\_CLK\_I)}$	Cycle time, TELE_CLK_I (2)	20			ns
2	$t_{w(TELE\_CLK\_I\_H)}$	Pulse duration, TELE_CLK_I high (2)	6			ns
3	$t_{w(TELE\_CLK\_I\_L)}$	Pulse duration, TELE_CLK_I low (2)	6			ns
	$f_{clock(HALF\_DSP\_CLK)}$	Clock frequency, ½ DSP_CLK (programmable clock source) (2)			50	MHz
4	$t_{c(HALF\_DSP\_CLK)}$	Cycle time, ½ DSP_CLK (2)	20			ns
5	$t_{w(HALF\_DSP\_CLK\_H)}$	Pulse duration, ½ DSP_CLK high (2)	7			ns
6	$t_{w(HALF\_DSP\_CLK\_L)}$	Pulse duration, ½ DSP_CLK low (2)	7			ns
	$f_{clock(TELE\_CLK\_O)}$	Clock frequency, TELE_CLK_O (2)			25	MHz
7	$t_{c(TELE\_CLK\_O)}$	Cycle time, TELE_CLK_O (2)	40			ns
			2	X (3)	4096	CLK_1 (4)
8	$t_{w(TELE\_CLK\_O\_H)}$	Pulse duration, TELE_CLK_O, high — When X is even	1	$(X/2)_t$	2048	CLK_1
		When X is odd		$(X/2)_t + 1$		
9	$t_{w(TELE\_CLK\_O\_L)}$	Pulse duration, TELE_CLK_O, low (2)	1	$(X/2)_t$	2048	CLK_1
10	$t_{w(TELE\_FS\_L)}$	Pulse duration, TELE_FS, low (2)	1		16,383	CLK_2 (5)
11	$t_{d(TELE\_FS)}$	Delay time, TELE_CLK_O↑ to TELE_FS↑/↓ (2)	1		15	ns

End of Table 5-53

1 Programmable clock source: Either TELE_CLK_I or ½ DSP_CLK may become the clock source, dependent on the state of the DSP_TELE (PCM_CTRL_2) register.

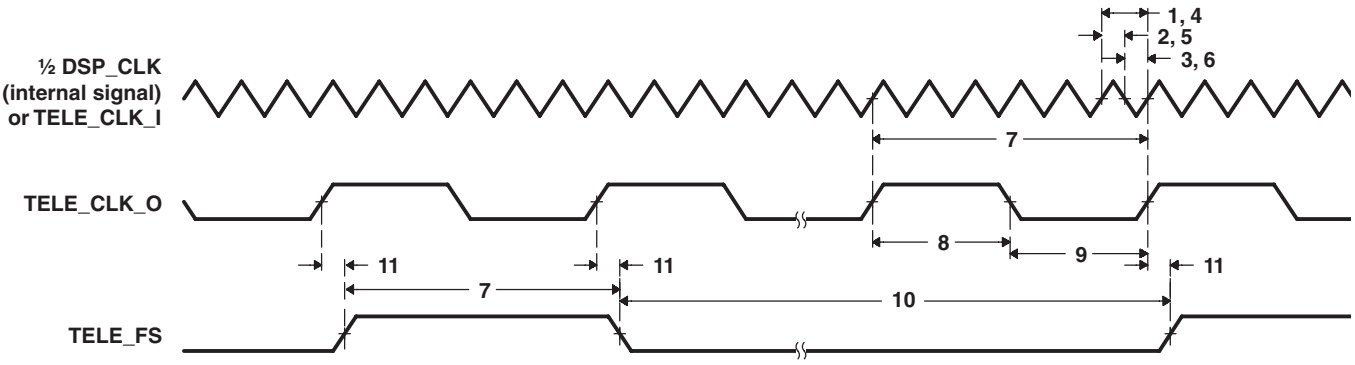
2 Specified by design

3 X: The total number of programmable clock source periods defined in the DSP_TELE (PCM_CTRL_1) register bits PCM_CLK_DIV. The value X is (PCM_CLK_DIV + 1), with zero invalid. In addition, the value $(X/2)_t$ is [½(PCM_CLK_DIV + 1)] truncated.

4 CLK_1: Clock periods based on the programmable clock source

5 CLK_2: Clock periods based on TELE_CLK_O

Figure 5-30 Telephony Interface PCM



5.11.2 Serial Port

Figure 5-31 and Figure 5-32 show a 4-bit serial data transfer, while valid data transfer sizes may be from 1 to 16 bits, dependent on the state of the DATA_LEN bits in the DSP_TELE (SERIAL_CTRL_1) register.

Table 5-54 Telephony Interface Serial Port Timing

See Figure 5-31 and Figure 5-32							
No.	**Description**			**Min**	**Typ**	**Max**	**Unit**
	$f_{clock(TELE\_DCLK)}$	Clock frequency, TELE_DCLK				25	MHz
1	$t_{c(TELE\_DCLK)}$	Cycle time, TELE_DCLK		40			ns
				2	X [1]	65,536	Clock [2]
2	$t_{w(TELE\_DCLK\_H)}$	Pulse duration, TELE_DCLK high	When X is even	1	$(X/2)_t$	32,782	Clock
			When X is odd	1	$(X/2)_t + 1$	32,782	
3	$t_{w(TELE\_DCLK\_L)}$	Pulse duration, TELE_DCLK low		1	$(X/2)_t$	32,782	Clock
4	$t_{d(TELE\_DO\_D)}$	Delay time, TELE_DCLK↑ to TELE_DO valid (driven)		1		15	ns
5	$t_{d(TELE\_DO\_R)}$	Delay time, TELE_DCLK↑ to TELE_DO invaild (released)		1		15	ns
6	$t_{d(TELE\_DO\_V)}$	Delay time, TELE_DCLK↑ to TELE_DO data bit invalid		1		15	ns
7	$t_{d(TELE\_DI)1}$ § [3]	Delay time, TELE_DI valid to TELE_DCLK↑		8			ns
8	$t_{d(TELE\_DO)1}$ §	Delay time, TELE_DO valid to TELE_DCLK↑		8			ns
9	$t_{d(TELE\_DI)2}$	Delay time, TELE_DI valid after TELE_DCLK↑ to TELE_DI invalid		4			ns
10	$t_{d(TELE\_DO)2}$	Delay time, TELE_DCLK↑ to TELE_DO invalid		4			ns
11	$t_{d(TELE\_CS\_A)}$	Delay time, TELE_DCLK↑ to $\overline{\text{TELE\_CS}}$↓		1		15	ns
12	$t_{d(TELE\_CS\_I)}$	Delay time, TELE_DCLK↑ to $\overline{\text{TELE\_CS}}$↑		1		15	ns
13	$t_{d(TELE\_DI\_ST)}$	Delay time, TELE_DCLK↑ to TELE_DI valid (read start)		1		15	ns
14	$t_{d(TELE\_DO\_ST)}$	Delay time, TELE_DCLK↑ to TELE_DO valid (read start)		1		15	ns
15	$t_{d(TELE\_DI\_SP)}$	Delay time, TELE_DCLK↑ to TELE_DI invalid (read stop)		1		15	ns
16	$t_{d(TELE\_DO\_SP)}$	Delay time, TELE_DCLK↑ to TELE_DO invalid (read stop)		1		15	ns
End of Table 5-54							

1 X: The total number of ½ DSP_CLK clock divider values defined in the DSP_TELE (SERIAL_CTRL_1) register bits CLK_DIV. The value X is (CLK_DIV + 1), with zero invalid. In addition, the value $(X/2)_t$ is [½(CLK_DIV + 1)] truncated.

2 Clock: One unit of clock period where the clock source is defined as ½ DSP_CLK

3 Bidirectional mode: The serial data input source on reads may be TELE_DI or TELE_DO, depending on the state of the D_MODE bit in the DSP_TELE (SERIAL_CTRL_1) register.

Figure 5-31 Telephony Interface Serial Port Write

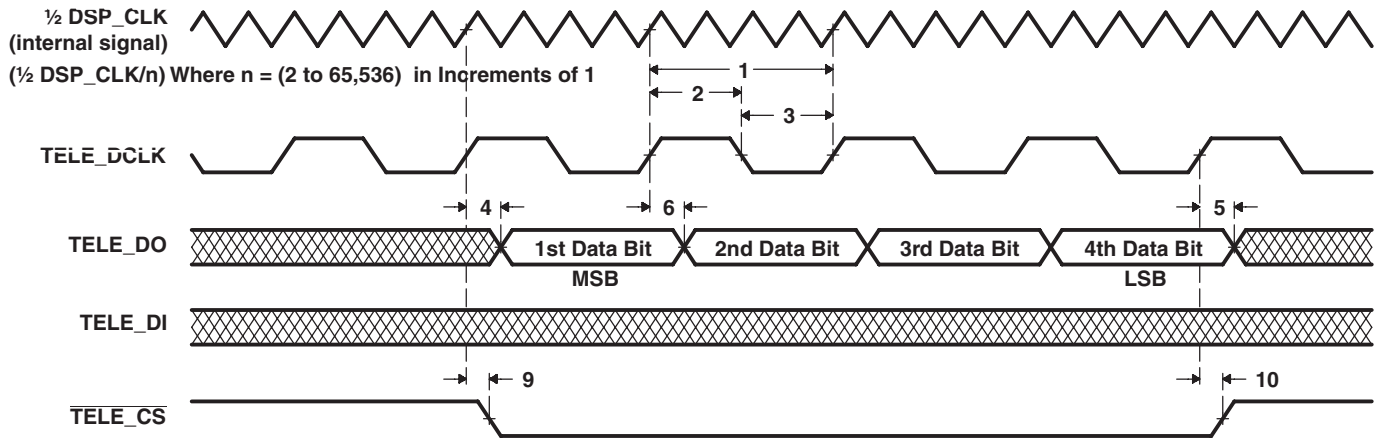
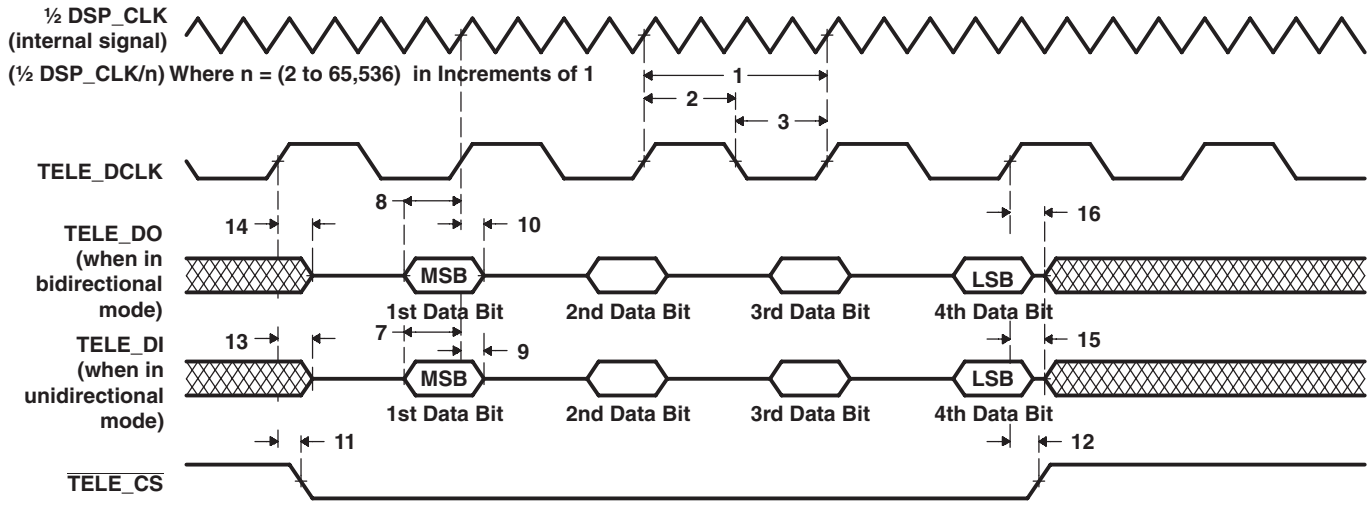


Figure 5-32 Telephony Interface Serial Port Read



5.11.3 Ring

Table 5-55 Telephony Interface Ring Timing [1]

See Figure 5-33

No.	Description		Min	Max	Unit
1	$t_{w(RING\_PRESCALE\_CLK)}$	Pulse duration, ring prescale clock period	2	8192	CLK_1 [2]
2	$t_{w(RING\_CLK)}$	Pulse duration, ring clock one-half period	1	65,535	CLK_2 [3]

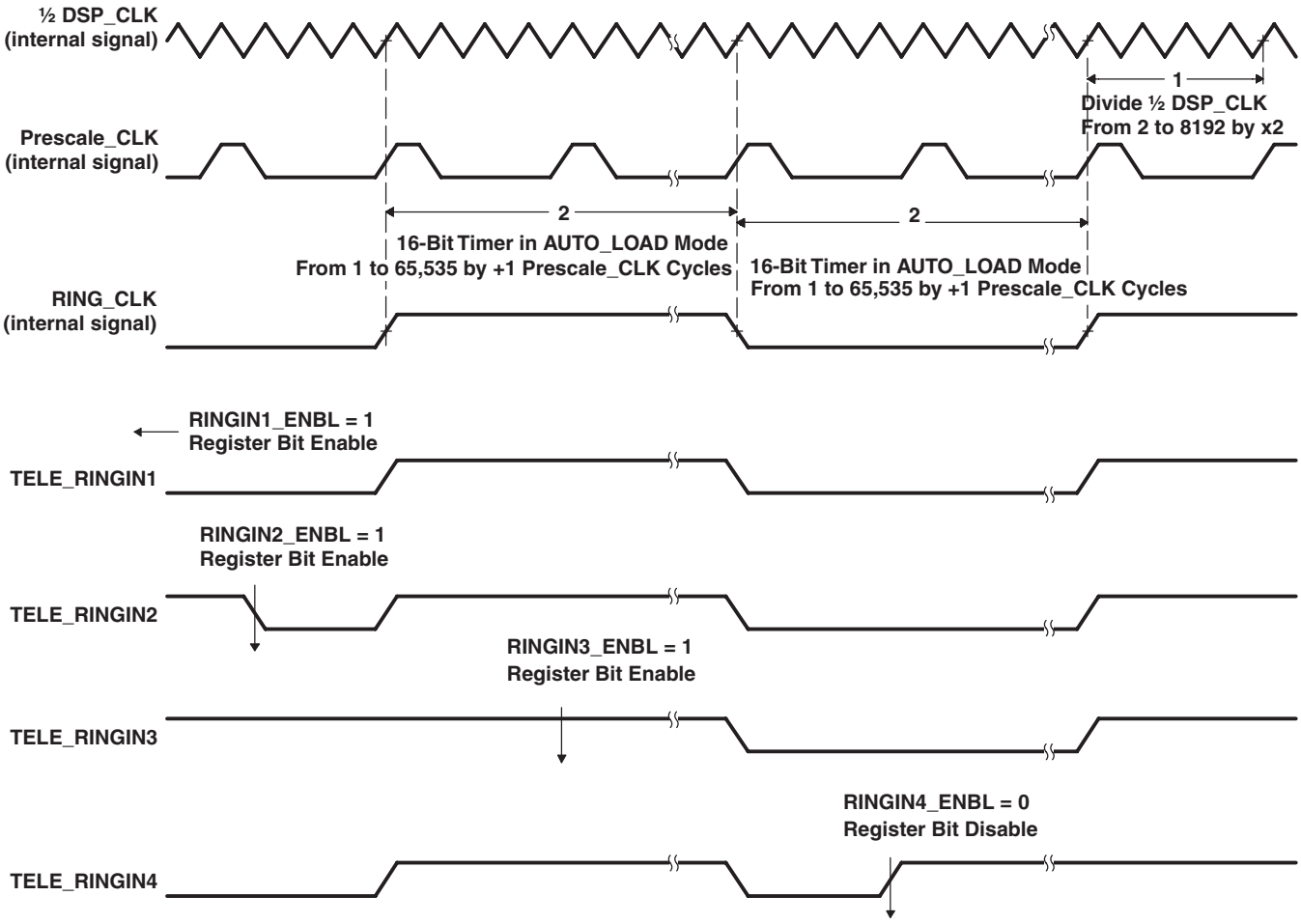
End of Table 5-55

1 TELE_RINGIN1/TELE_RINGIN2/TELE_RINGIN3/TELE_RINGIN4 signals are enabled through DSP_TELE(RINGIN).

2 CLK_1: One ½ DSP_CLK period

3 CLK_2: One ring prescalar clock period defined above. The ring prescalar clock is programmed through the universal timer register DSP_TELE (CTRL). The ring clock is programmed through the universal timer register DSP_TELE (LOAD), with a value larger than zero.

Figure 5-33 Telephony Interface Ring



5.12 UART Interface Timing

Table 5-56 UART Timing [1]

See Figure 5-34					
No.	**Description**		**Min**	**Max**	**Unit**
	BAUD	BAUD rate [2] [3]	1200	256,000	BAUD
	$f_{clock(DIV\_CLK)}$	Clock frequency, DIV_CLK [2] [4]		62.5	MHz
1	$t_{c(DIV\_CLK)}$	Cycle time, divider clock [2]	16		ns
2	$t_{d(UART\_TX\_P)}$	Delay time, UART_TX pause between stop and start UART_CTS transfers [2]	$t_c \times 0$		ns
3	$t_{d(UART\_CTS\_I)}$	Delay time, UART_CTS↑ to middle of stop bit [2]		16	ns
4	$t_{d(UART\_CTS\_A)}$	Delay time, UART_CTS↓ to UART_TX start bit↓ [2]		$t_c \times 25$	ns
5	$t_{d(UART\_RX\_P)}$	Delay time, UART_RX pause between stop and start UART_RTS transfers [2]	$t_c \times 0$		ns
6	$t_{d(UART\_RTS\_I)}$	Delay time, middle of stop bit on UART_RX (RX_FIFO trigger active) to UART_RTS↑ [2]		$t_c \times 3$	ns
7	$t_{d(UART\_RTS\_A)}$	Delay time, RX FIFO trigger reset to UART_RTS↓ [2]		$t_c \times 4$	ns
End of Table 5-56					

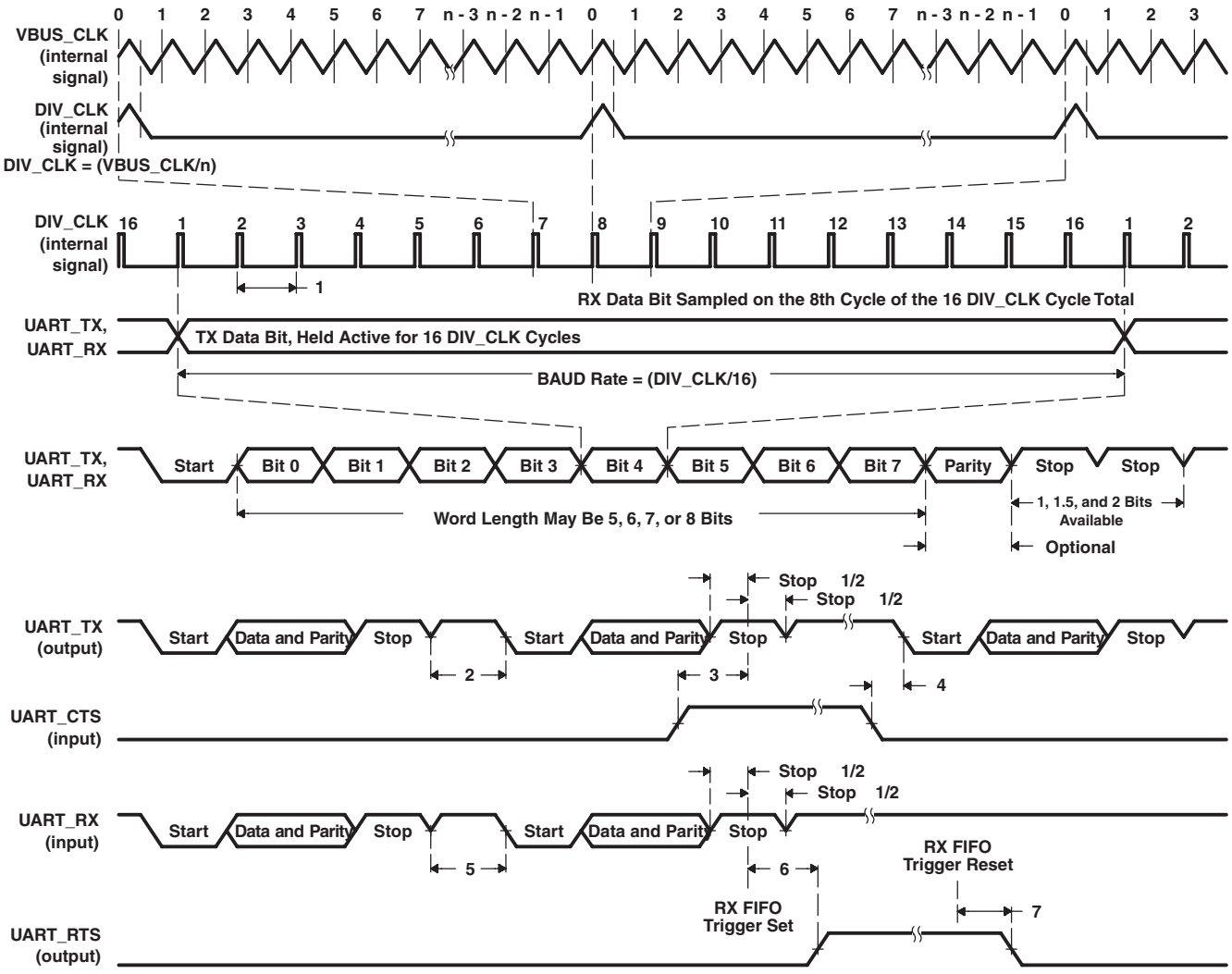
1 Auto flow: Through the UART (MODEM_CTRL) register, the UART may be set for auto flow. In auto-flow mode, the UART may transmit data on UART_TX whenever UART_CTS is active. In addition, the UART must be ready to receive data on UART_RX, as long as the UART is holding UART_RTS active.

2 Specified by design

3 BAUD rate: BAUD rate is created from the DIV_CLK, further divided by the fixed value 16.

4 Divider clock: This DIV_CLK value is created by dividing the VBUS_CLK frequency by the DLH and DLL values found in the UART (DIV_LATCH_LSB) and UART (DIV_LATCH_MSB) register set.

Figure 5-34 UART



5.13 LCD Interface Timing

This section provides timing information for the following LCD modes:

- "LCD Interface Display Driver (LIDD) Mode" on page 137
- "Raster Mode" on page 145

5.13.1 LCD Interface Display Driver (LIDD) Mode

Each LIDD-mode chip select is provided with a control register that allows individual adjustment of the write timing parameters (W_SU, W_STROBE, and W_HOLD), read timing parameters (R_SU, R_STROBE, and R_HOLD), and chip select delay timing (CS_DELAY).

- E0 provided on LCD_BIAS_E0, register LCD (LIDD_CS0_CONFIG)
- E1 provided on LCD_E1, register LCD (LIDD_CS1_CONFIG)

This section provides timing information for the following operations:

- "LCD LIDD Mode Timing" on page 138
- "Character Display HD44780 Write" on page 138
- "Character Display HD44780 Read" on page 139
- "Micro-Interface Graphic Display 6800 Write" on page 140
- "Micro-Interface Graphic Display 6800 Read" on page 141
- "Micro-Interface Graphic Display 6800 Status" on page 142
- "Micro-Interface Graphic Display 8080 Write" on page 143
- "Micro-Interface Graphic Display 8080 Read" on page 144
- "Micro-Interface Graphic Display 8080 Status" on page 145

Table 5-57 LCD LIDD Mode Timing

See Figure 5-35 through Figure 5-42					
No.	**Description**		**Min**	**Max**	**Unit**
	$f_{clock(LIDD\_CLK)}$	Clock frequency, LIDD_CLK (1)		62.5	MHz
1	$t_{c(LIDD\_CLK)}$	Cycle time, LIDD_CLK	16		ns
2	$t_{w(LIDD\_CLK\_H)}$	Pulse duration, LIDD_CLK high	6		ns
3	$t_{w(LIDD\_CLK\_L)}$	Pulse duration, LIDD_CLK low	6		ns
4	$t_{d(LCD\_D\_V)}$	Delay time, LIDD_CLK↑ to LCD_D[15:00] valid (write)	1	7	ns
5	$t_{d(LCD\_D\_I)}$	Delay time, LIDD_CLK↑ to LCD_D[15:00] invalid (write)	1	7	ns
6	$t_{d(LCD\_E\_A)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_BIAS_E0 or LCD_E1↓ (2)	1	7	ns
7	$t_{d(LCD\_E\_I)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_BIAS_E0 or LCD_E1↑ (2)	1	7	ns
8	$t_{d(LCD\_A\_A)}$	Delay time, LIDD_CLK↑ to LCD_VSYNC_A↓	1	7	ns
9	$t_{d(LCD\_A\_I)}$	Delay time, LIDD_CLK↑ to LCD_VSYNC_A↑	1	7	ns
10	$t_{d(LCD\_W\_A)}$	Delay time, LIDD_CLK↑ to $\overline{\text{LCD\_HSYNC\_W}}$↓	1	7	ns
11	$t_{d(LCD\_W\_I)}$	Delay time, LIDD_CLK↑ to $\overline{\text{LCD\_HSYNC\_W}}$↑	1	7	ns
12	$t_{d(LCD\_STRB\_A)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_PIXEL_STRB↑	1	7	ns
13	$t_{d(LCD\_STRB\_I)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_PIXEL_STRB↓	1	7	ns
14	$t_{d(LCD\_D\_Z)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_D[15:00] in 3-state Z	1	7	ns
15	$t_{d(Z\_LCD\_D)}$	Delay time, LIDD_CLK↑ (LCD_E1)↑ to LCD_D[15:00] (valid from 3-state Z)	1	7	ns
16	$t_{su(LCD\_D)}$	Setup time, LCD_D[15:00] valid before LIDD_CLK (LCD_E1)↑	7		ns
17	$t_{h(LCD\_D)}$	Hold time, LCD_D[15:00] valid after LIDD_CLK (LCD_E1)↑	2		ns
End of Table 5-57					

1 The LIDD clock is available on LCD_E1 when operating the LIDD in 6800 synchronous mode and 8080 synchronous mode, but is not available externally in HD44780 mode. LIDD mode selects are provided in the LCD (LIDD_CTRL) register.

2 Control signal polarity: The active polarity of the control signals (LCD_BIAS_E0, LCD_E1, LCD_VSYNC_A, $\overline{\text{LCD\_HSYNC\_W}}$, and LCD_PIXEL_STRB) is individually programmable in LIDD mode through the LCD (LIDD_CTRL) register.

Figure 5-35 Character Display HD44780 Write

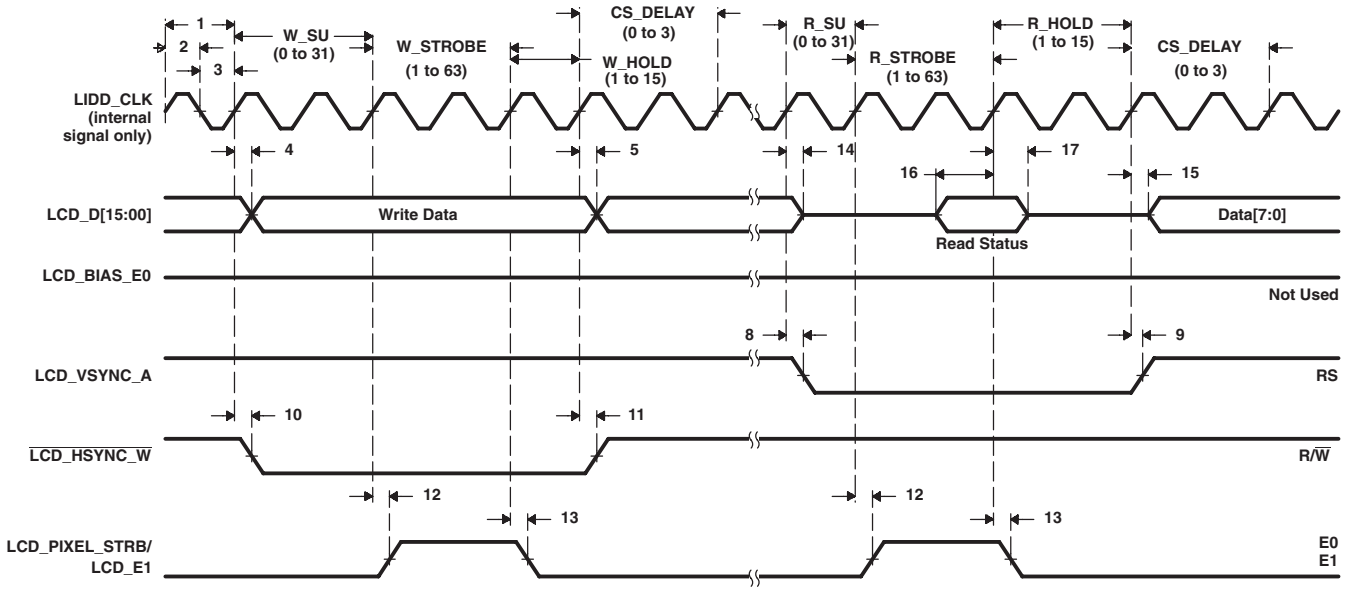


Figure 5-36 Character Display HD44780 Read

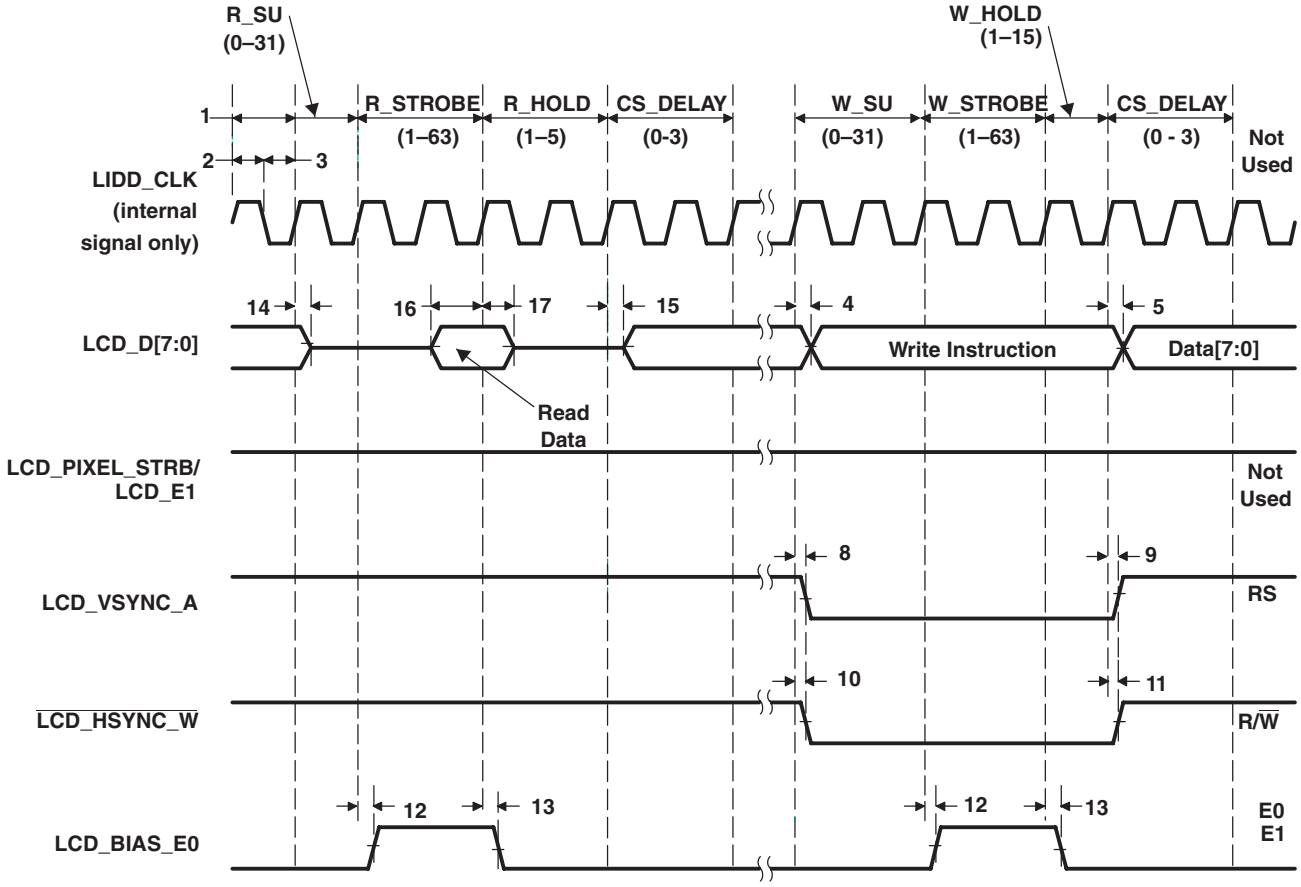


Figure 5-37 Micro-Interface Graphic Display 6800 Write

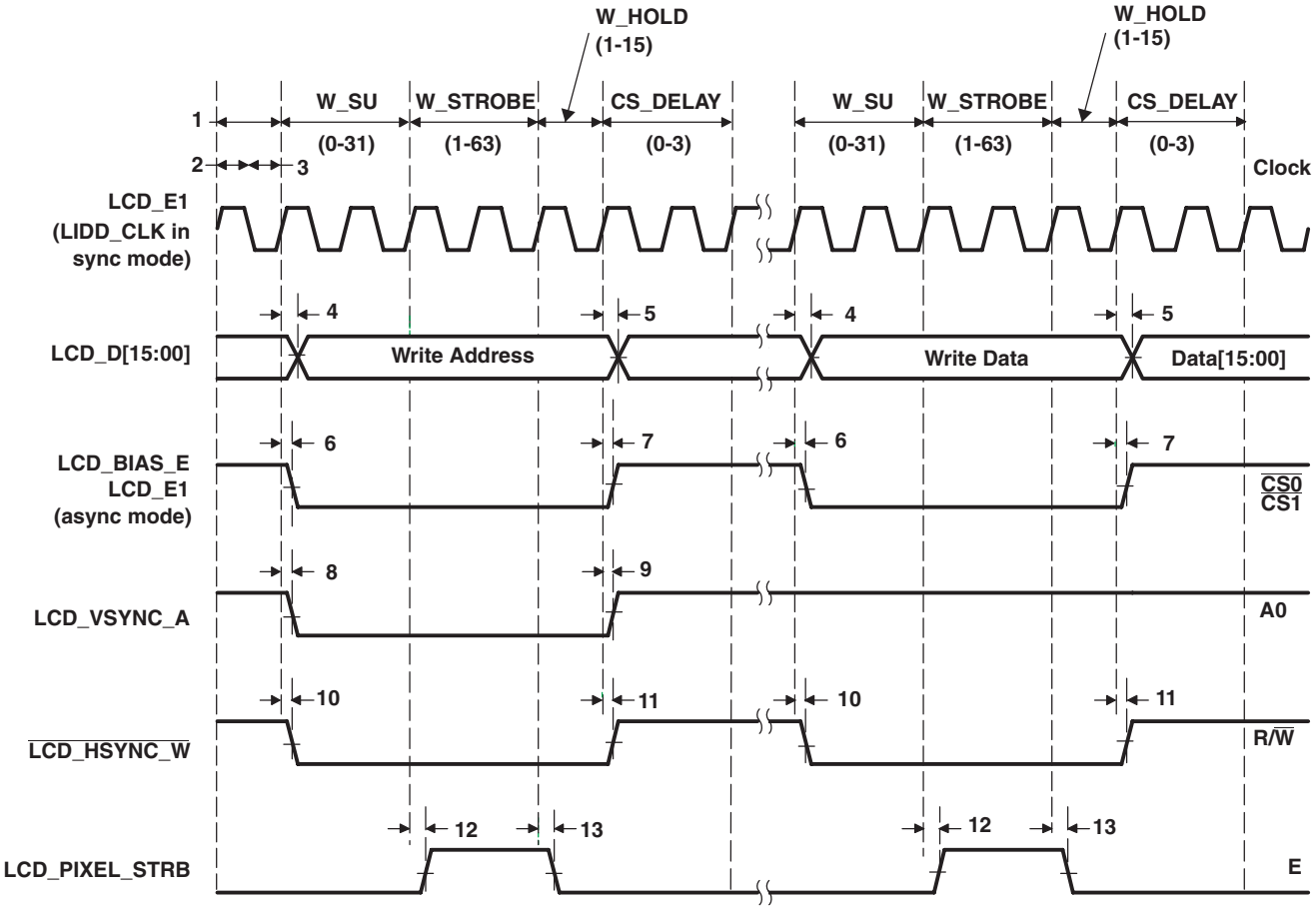


Figure 5-38 Micro-Interface Graphic Display 6800 Read

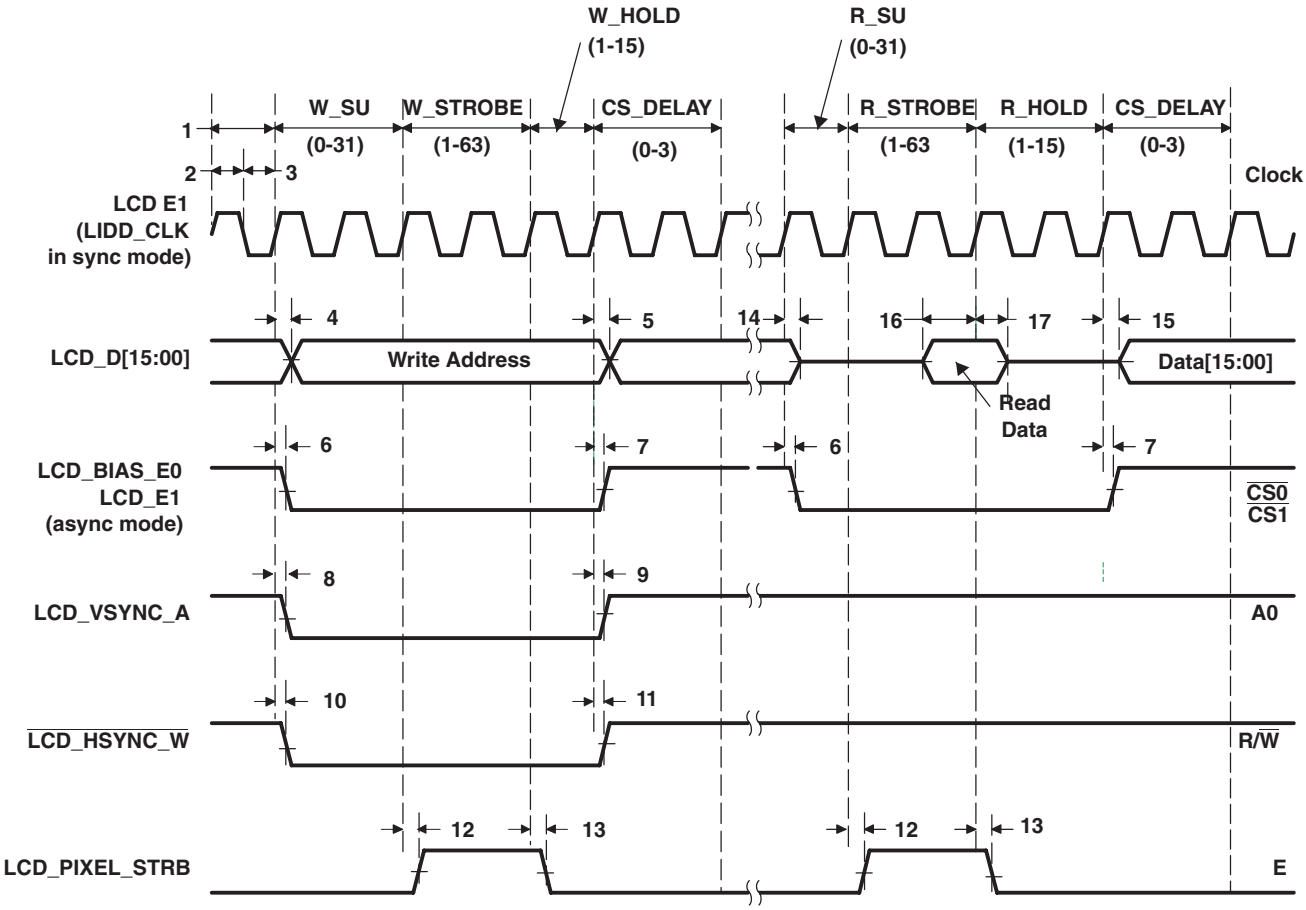


Figure 5-39 Micro-Interface Graphic Display 6800 Status

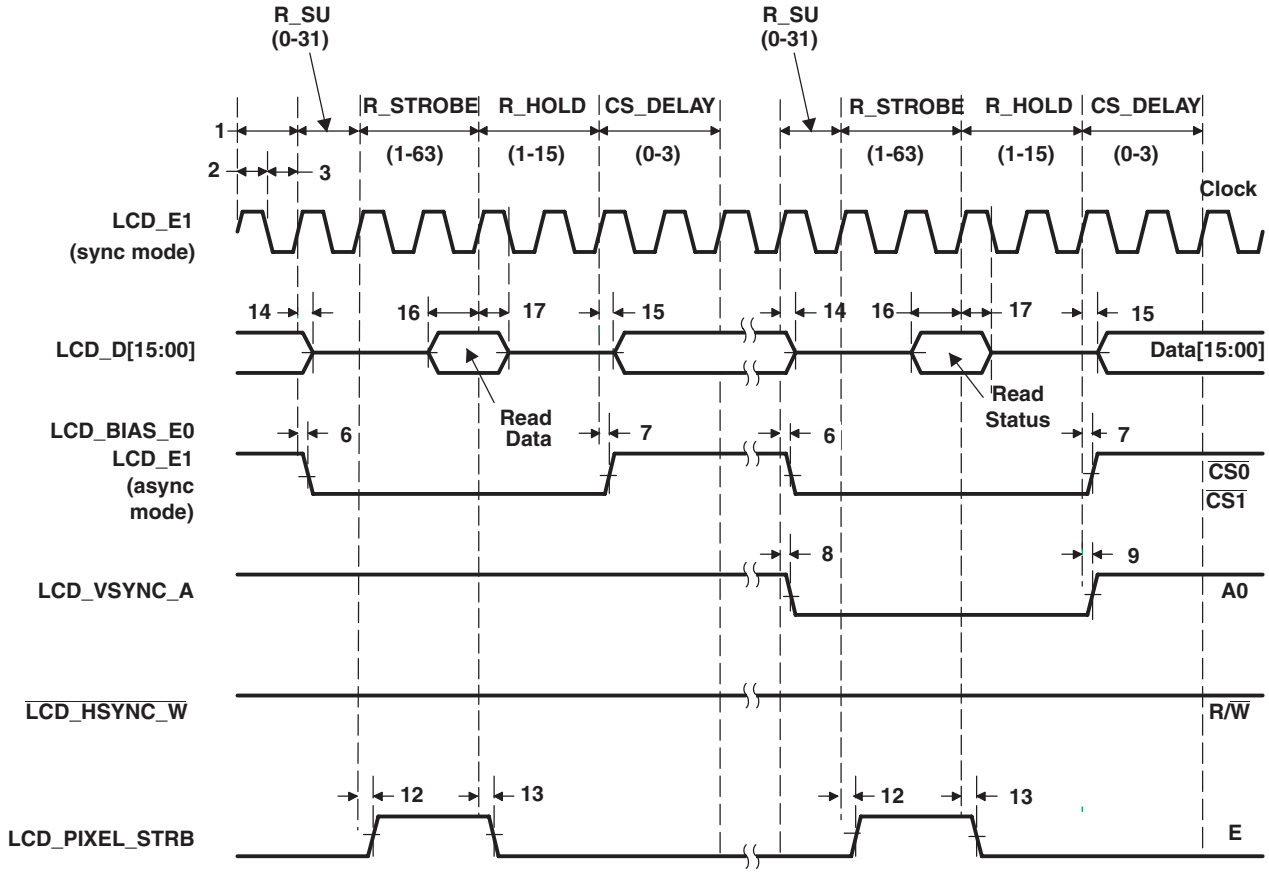


Figure 5-40 Micro-Interface Graphic Display 8080 Write

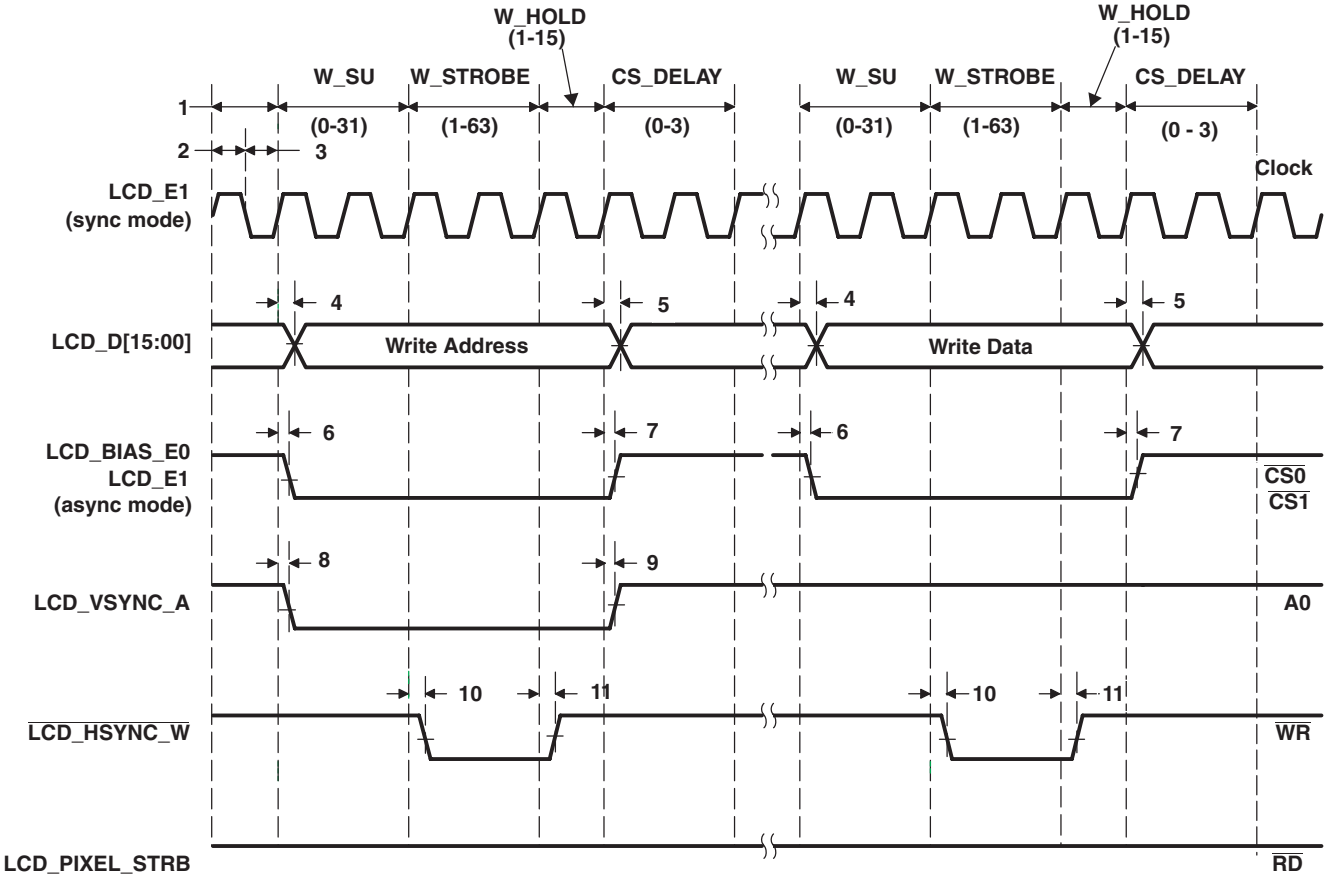


Figure 5-41 Micro-Interface Graphic Display 8080 Read

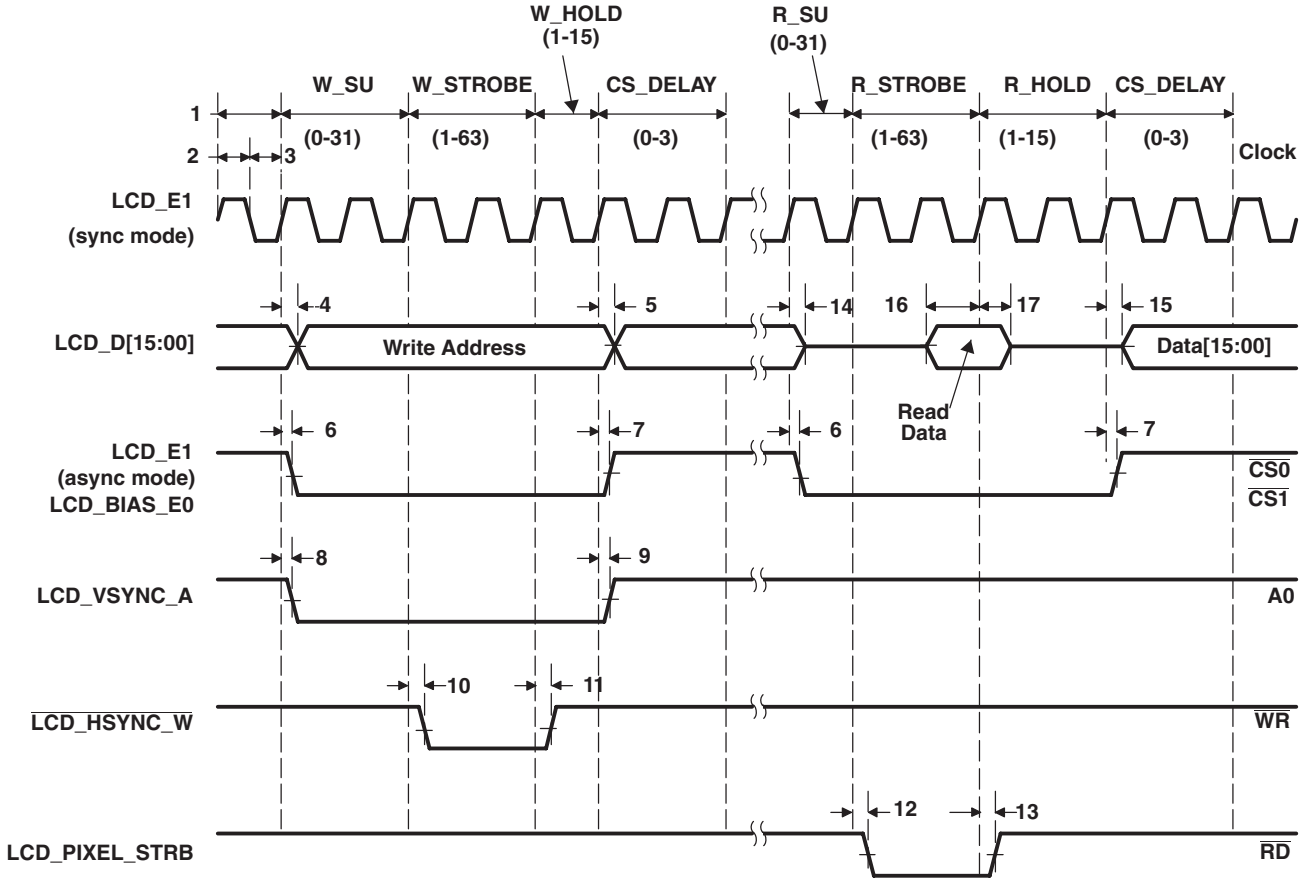
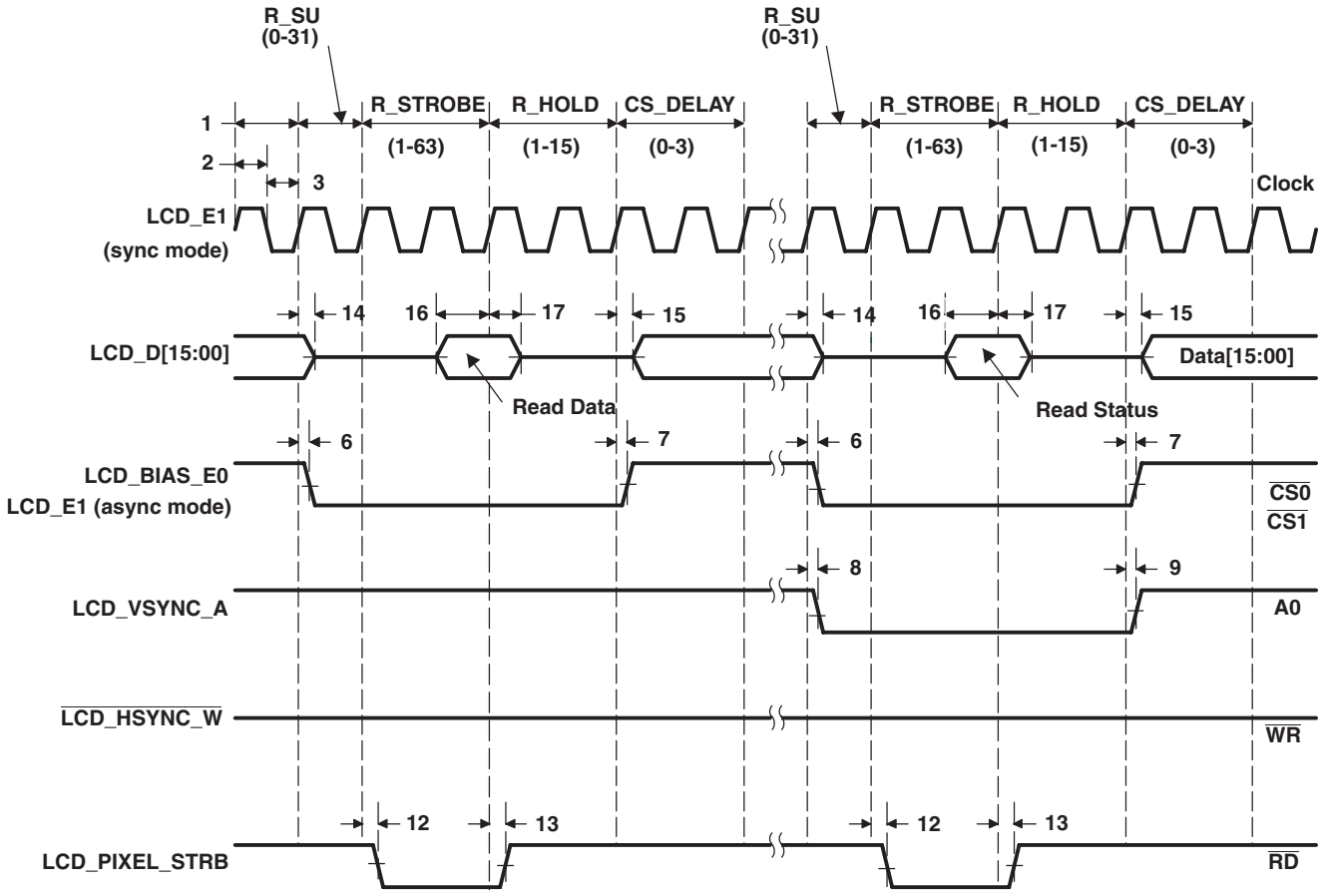


Figure 5-42 Micro-Interface Graphic Display 8080 Status



5.13.2 Raster Mode

This section provides timing information for the following topics:

- "LCD Raster Mode Timing" on page 146
- "LCD Raster Mode Display Format" on page 147
- "LCD Raster Mode, Active" on page 148
- "LCD Raster Mode, Passive" on page 149
- "LCD Raster Mode Control Signal Activation" on page 150
- "LCD Raster Mode Control Signal Deactivation" on page 151

Table 5-58 LCD Raster Mode Timing

See Figure 5-43 through Figure 5-47					
No.	**Description**		**Min**	**Max**	**Unit**
	$f_{clock(PIXEL\_CLK)}$	Clock frequency, pixel clock (1)		31.25	MHz
1	$t_{c(PIXEL\_CLK)}$	Cycle time, pixel clock	32		ns
2	$t_{w(PIXEL\_CLK\_H)}$	Pulse duration, pixel clock high (2)	10		ns
3	$t_{w(PIXEL\_CLK\_L)}$	Pulse duration, pixel clock low	10		ns
4	$t_{d(LCD\_D\_V)}$	Delay time, LCD_PIXEL_STRB↑ to LCD_D[15:00] valid (write) (3)	1	7	ns
5	$t_{d(LCD\_D\_IV)}$	Delay time, LCD_PIXEL_STRB↑ to LCD_D[15:00] invalid (write)	1	7	ns
6	$t_{d(LCD\_BIAS\_A)}$	Delay time, LCD_PIXEL_STRB↓ to LCD_BIAS_E0↑	1	7	ns
7	$t_{d(LCD\_BIAS\_I)}$	Delay time, LCD_PIXEL_STRB↓ to LCD_BIAS_E0↓	1	7	ns
8	$t_{d(LCD\_VSYNC\_A)}$	Delay time, LCD_PIXEL_STRB↓ to LCD_VSYNC_A↑	1	7	ns
9	$t_{d(LCD\_VSYNC\_I)}$	Delay time, LCD_PIXEL_STRB↓ to LCD_VSYNC_A↓	1	7	ns
10	$t_{d(LCD\_HSYNC\_A)}$	Delay time, LCD_PIXEL_STRB↑ to $\overline{\text{LCD\_HSYNC\_W}}$↑	1	7	ns
11	$t_{d(LCD\_HSYNC\_I)}$	Delay time, LCD_PIXEL_STRB↑ to $\overline{\text{LCD\_HSYNC\_W}}$↓	1	7	ns
End of Table 5-58					

1 The pixel clock always is available on LCD_PIXEL_STRB. In addition, the polarity of this clock may be inverted while in raster mode, producing timing delay from the opposite edge of the clock. This may be accomplished through the LCD (RASTER_TIMING_2) register.

2 The active polarity of the control signals (LCD_BIAS_E0, LCD_VSYNC_A, and $\overline{\text{LCD\_HSYNC\_W}}$) is individually programmable in raster mode through the LCD (RASTER_TIMING_2) register.

3 The activation edge of the control signals LCD_VSYNC_A and $\overline{\text{LCD\_HSYNC\_W}}$ may be programmed to either the rising or falling edge of the pixel clock through the LCD (RASTER_TIMING_2) register. In Figure 5-43 through Figure 5-47, all signal polarity and activation edges are based on the default LCD (RASTER_TIMING_2) register settings.

Frame-to-frame timing is derived through the following parameters in the LCD (RASTER_TIMING_1) register:

- Vertical front porch (VFP)
- Vertical sync pulse width (VSW)
- Vertical back porch (VBP)
- Lines per panel (LPP)

Line-to-line timing is derived through the following parameters in the LCD (RASTER_TIMING_0) register:

- Horizontal front porch (HFP)
- Horizontal sync pulse width (HSW)
- Horizontal back porch (HBP)
- Pixels per panel (PPL)

LCD_BIAS_E0 timing is derived through the following parameter in the LCD (RASTER_TIMING_2) register:

- AC bias frequency (ACB)

The display format produced in raster mode is shown in Figure 5-43. An entire frame is delivered one line at a time. The first line delivered starts at data pixel (1, 1) and ends at data pixel (P, 1). The last line delivered starts at data pixel (1, L) and ends at data pixel (P, L). The beginning of each new frame is denoted by the activation of I/O signal LCD_VSYNC_A. The beginning of each new line is denoted by the activation of I/O signal LCD_HSYNC_W.

Figure 5-43 LCD Raster Mode Display Format

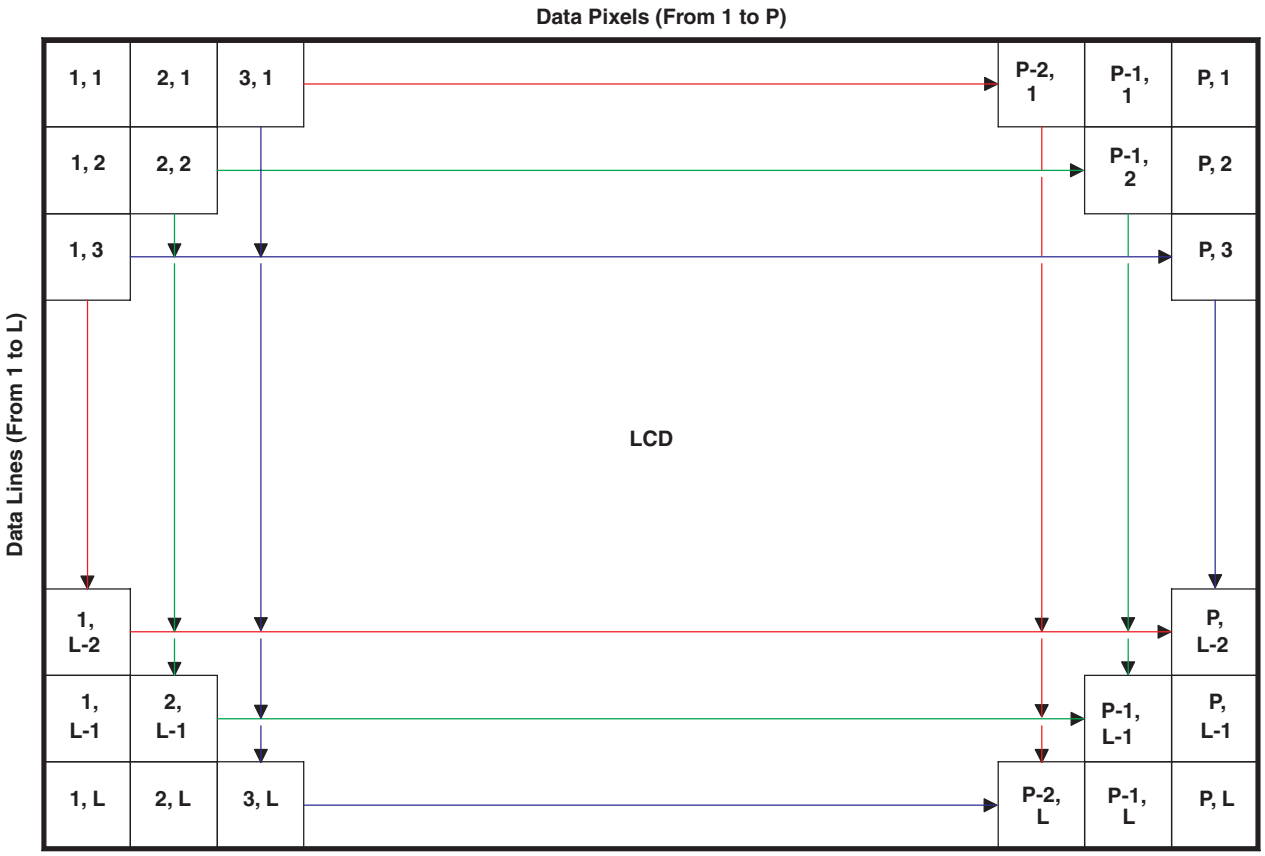


Figure 5-44 LCD Raster Mode, Active

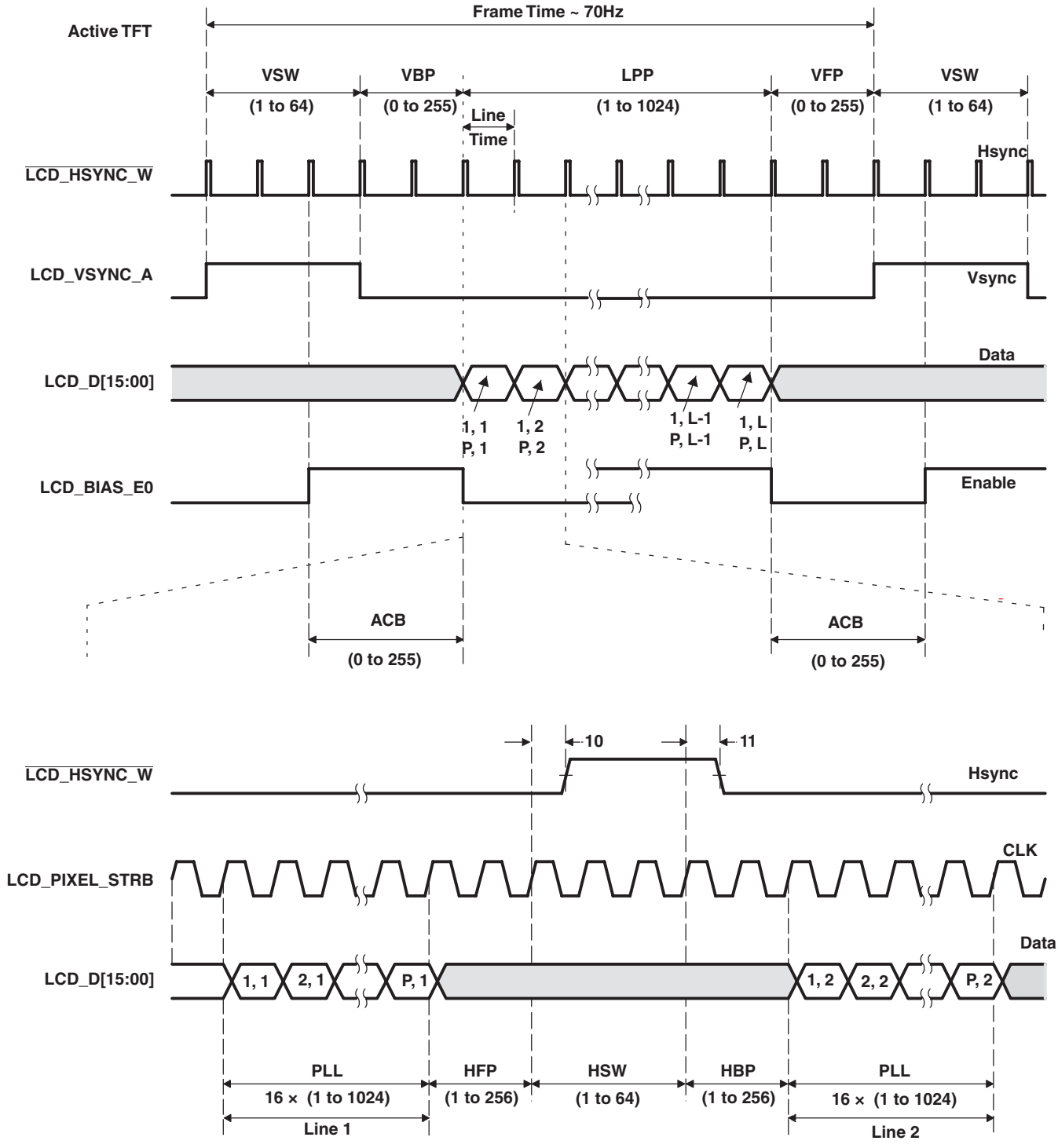


Figure 5-45 LCD Raster Mode, Passive

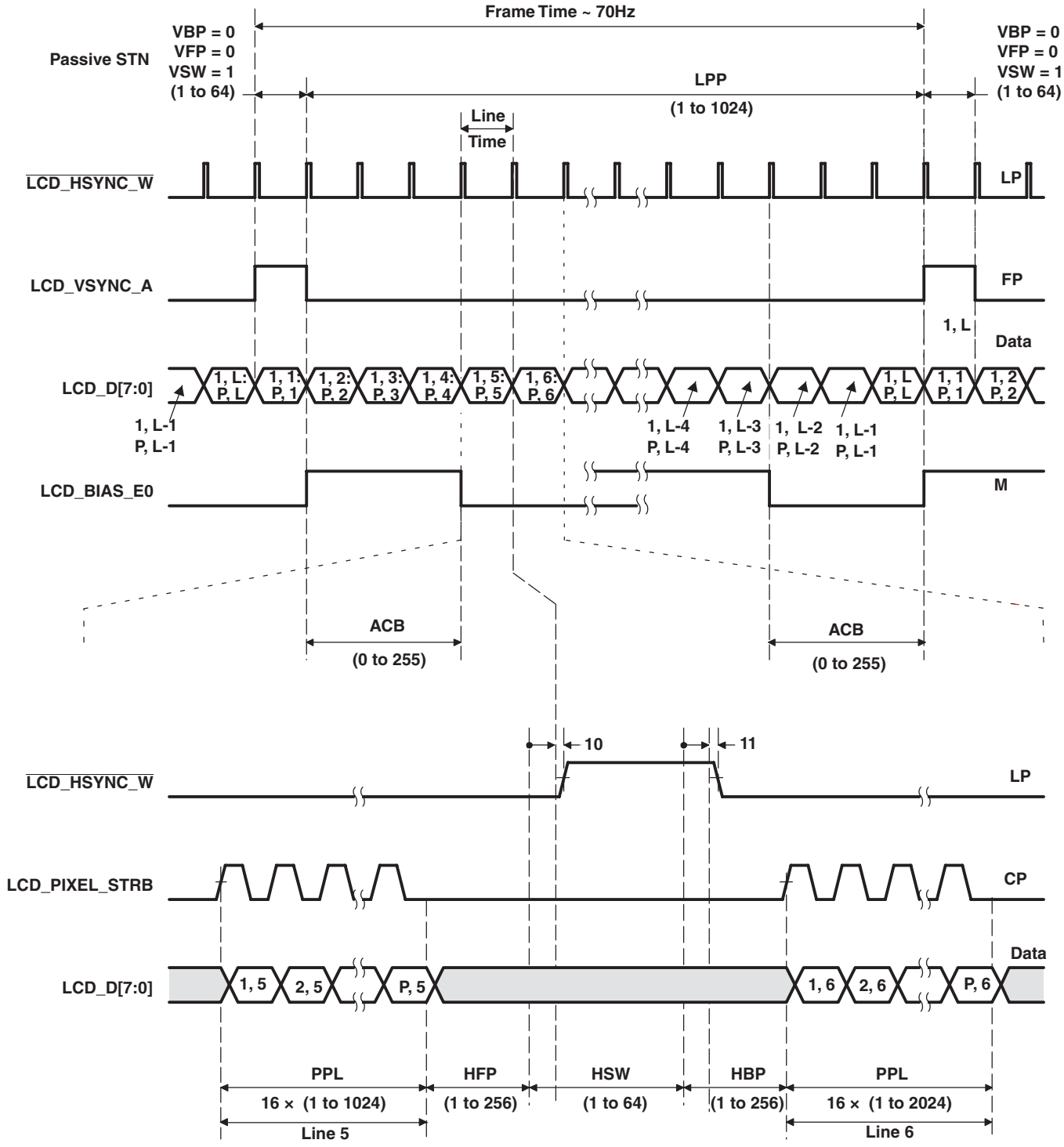


Figure 5-46 LCD Raster Mode Control Signal Activation

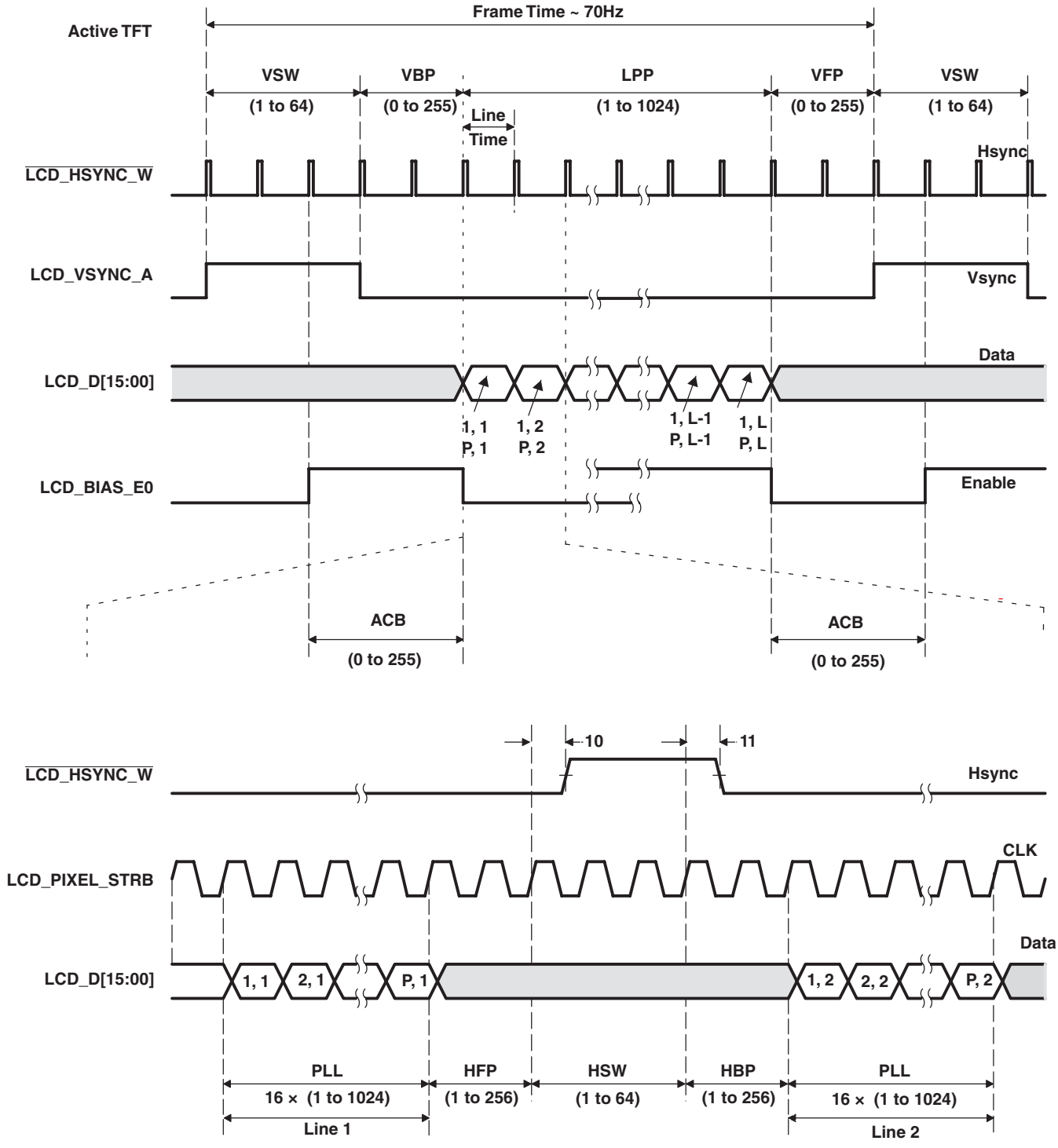
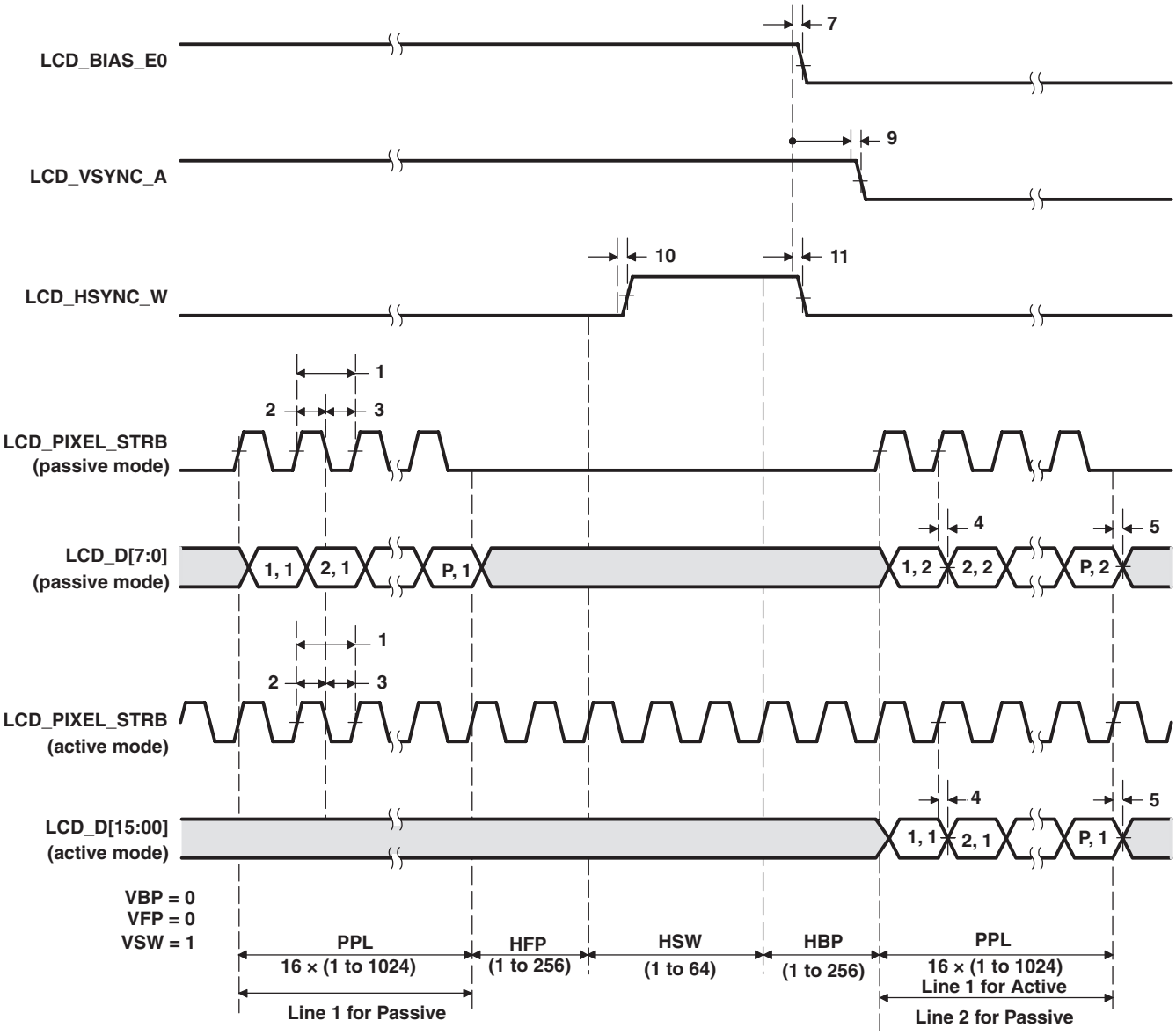


Figure 5-47 LCD Raster Mode Control Signal Deactivation



5.14 SSP Timing

The SSP unit contains two flexible sequencer engines and five control signals to support a wide variety of serial interfaces. In the following timing diagrams, a simple serial port interface (SPI) is chosen to present the SSP timing. The timing defined by the SPI is identical to any other serial interface type. In addition, the signals SSPx, SSPy, and SSPz may be individually configured to be any one of the five control signals (SSP0, SSP1, SSP2, SSP3, or SSP4).

Table 5-59 SSP Timing

See Figure 5-48 through Figure 5-51					
No.	**Description**		**Min**	**Max**	**Unit**
	$f_{clock(SSP\_CLK)}$	Clock frequency, SSP_CLK (1)		31.25	MHz
1	$t_{c(SSP\_CLK)}$	Cycle time, SSP_CLK	32		ns
2	$t_{w(SSP\_CLK\_H)}$	Pulse duration, SSP_CLK high	12		ns
3	$t_{w(SSP\_CLK\_L)}$	Pulse duration, SSP_CLK low	12		ns
4	$t_{d(SSP\_D\_D)}$	Delay time, SSP_CLK↑↓ to data drive (to valid) (2)	1	9	ns
5	$t_{d(SSP\_D\_R)}$	Delay time, SSP_CLK↓ to data release (to invalid) (2)	1	9	ns
6	$t_{d(SSP\_DO)}$	Delay time, SSP_CLK↓ to data bit shift out valid (2)	1	9	ns
7	$t_{d(SSP\_DI)}$	Delay time, data bit shift in before SSP_CLK↓ (3)	1	9	ns
8	$t_{d(SSP\_DI)}$	Delay time, SSP_CLK↓ to 3-state Z (3)	1	9	ns
9	$t_{d(SSP\_E\_A)}$	Delay time, SSP_CLK↑ to SSPz↓	8		ns
10	$t_{d(SSP\_E\_I)}$	Delay time, SSP_CLK↑ to SSPz↑	4		ns
End of Table 5-59					

1 This internal clock signal drives the SSP engine and is created from the VBUS_CLK after being divided by two clock dividers. External visibility of this clock signal is dependent on the sequencer program.

2 The serial data exiting the TNETV1056 may be configured to delay one VBUS_CLK cycle (see Figure 5-50) through the DELAY_OUT control bit in either the SSP (CONFIG_1_PORT_0) or SSP (CONFIG_1_PORT_1) register.

3 The serial data entering the TNETV1056 may be configured to load into the deserializer ½ SSP_CLK cycle early (see Figure 5-51) through the EARLY_IN control bit in either the SSP (CONFIG_1_PORT_0) or SSP (CONFIG_1_PORT_1) register.

Figure 5-48 Serial Port Data Out

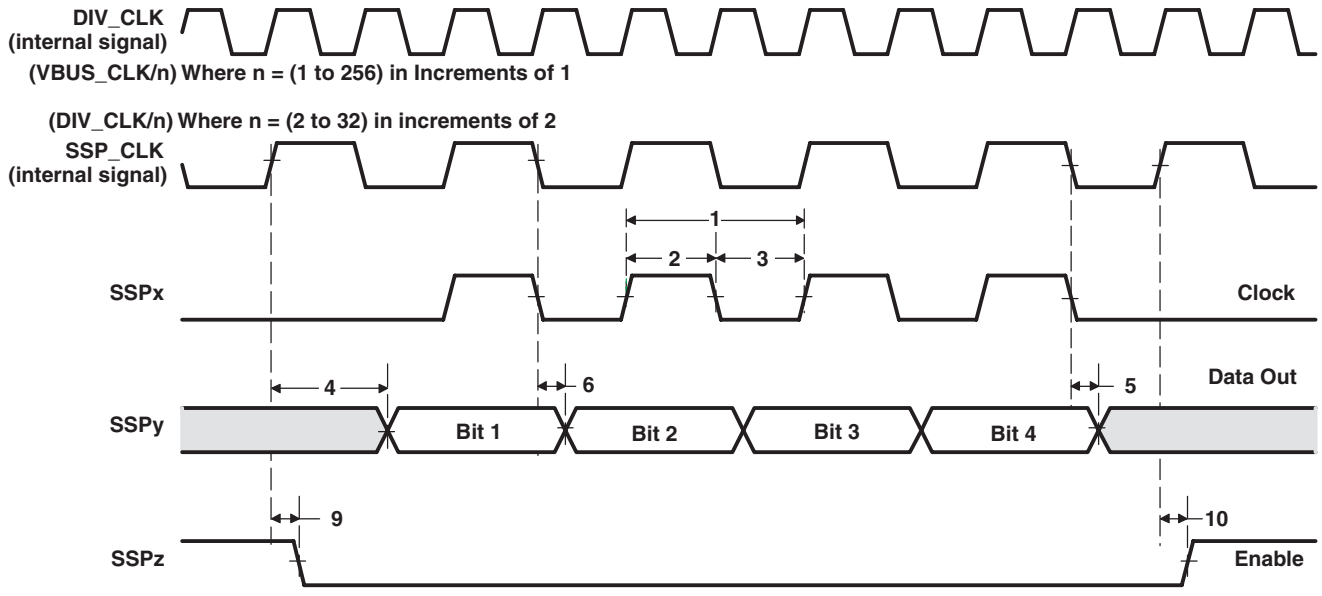


Figure 5-49 Serial Port Data In

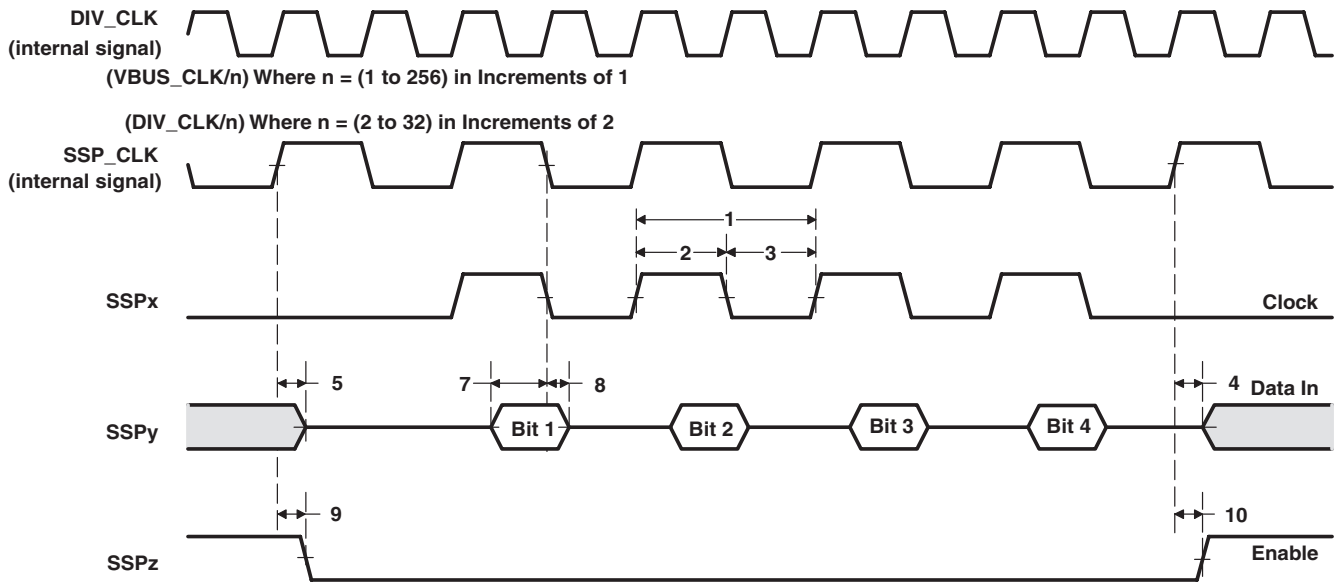


Figure 5-50 Serial Port Data Out Delay

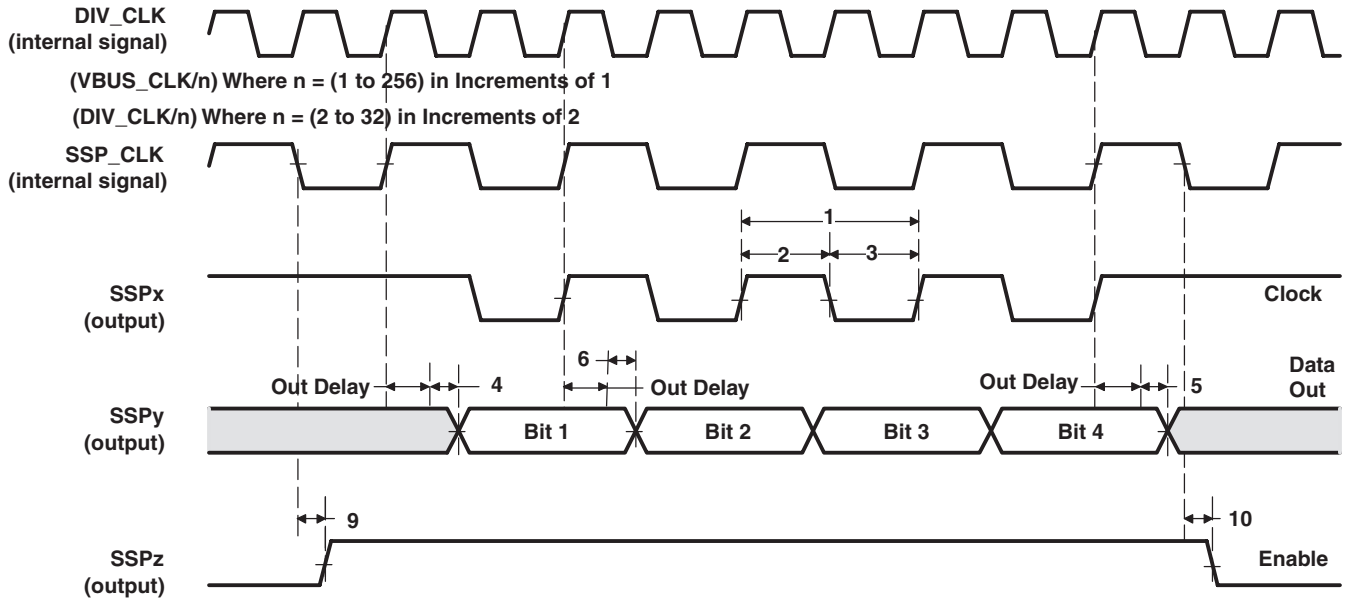
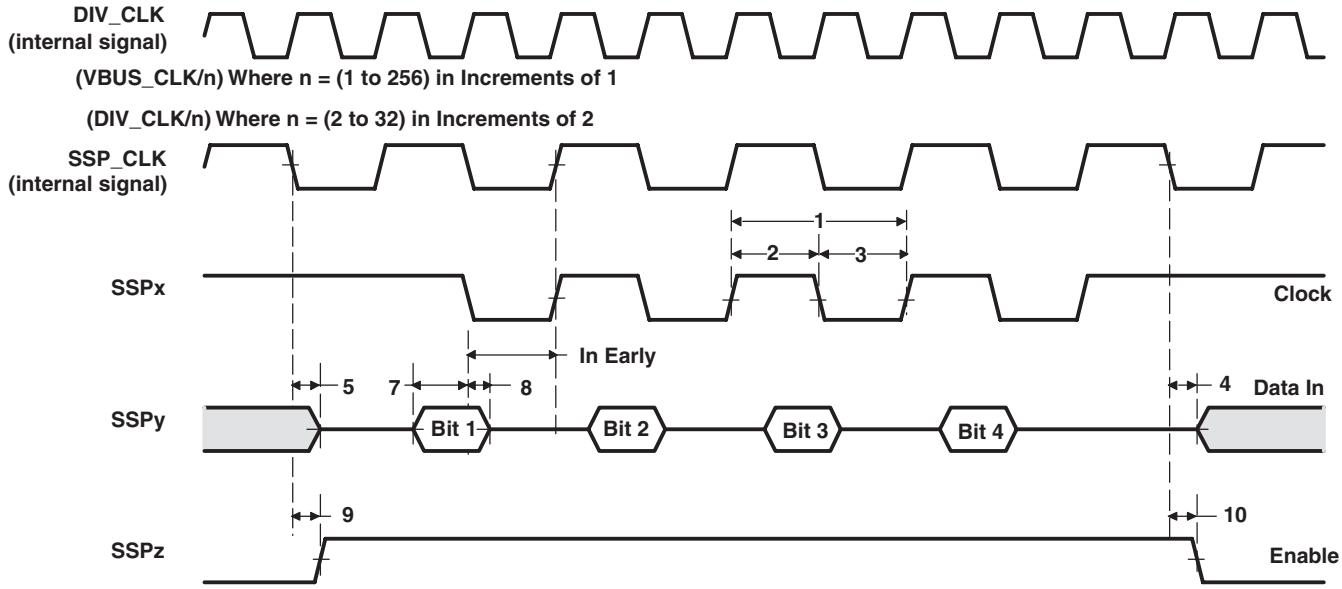


Figure 5-51 Serial Port Data In Early



5.15 VLYNQ Interface Timing

There is one five-terminal VLYNQ unit within the TNETV1056.

Table 5-60 VLYNQ Timing Requirements (1) (2)

See Figure 5-52					
No.	**Description**		**Min**	**Max**	**Unit**
	$f_{clock(VLYNQ\_CLK)}$	Clock frequency, VLYNQ5_CLK		62.5	MHz
1	$t_{c(VLYNQ\_CLK)}$	Cycle time, VLYNQ5_CLK (input mode)	16		ns
2	$t_{w(VLYNQ\_CLK\_H)}$	Pulse duration, VLYNQ5_CLK high (input mode) (3)	3.6		ns
3	$t_{w(VLYNQ\_CLK\_L)}$	Pulse duration, VLYNQ5_CLK low (input mode) (3)	3.6		ns
4	$t_{r(VRCKR)}$	Rise time, VLYNQ5_RX_D[1:0] and VLYNQ5_CLK (input mode) (3)		3.0	ns
5	$t_{f(VRCKF)}$	Fall time, VLYNQ5_RX_D[1:0] and VLYNQ5_CLK (input mode) (3)		3.0	ns
6	$t_{d(VRV-VCKH)}$	Delay time, VLYNQ5_RX_D[1:0] valid to VLYNQ5_CLK	1		ns
7	$t_{d(VCKH-VRV)}$	Delay time, VLYNQ5_CLK to VLYNQ5_RX_D[1:0]	2		ns
End of Table 5-60					

1 The VLYNQ clock can be sourced internally or externally through the configuration bit CLK_DIR in the VLYNQ5 (CTRL) register. If sourced internally, this clock is based on the VBUSP_CLK.

2 See section 4 of Texas Instruments application report SPRA956, Circuit-Board Design Guidelines for VLYNQ™ Devices, to determine how to analyze VLYNQ timing.

3 Specified by design

Table 5-61 VLYNQ Switching Characteristics (1) (2)

See Figure 5-52					
No.	**Description**		**Min**	**Max**	**Unit**
	$f_{clock(VLYNQ\_CLK)}$	Clock frequency, VLYNQ5_CLK		62.5	MHz
1	$t_{c(VLYNQ\_CLK)}$	Cycle time, VLYNQ5_CLK (output mode)	16		ns
	$t_{j(VLYNQ\_CLK)}$	Cycle to cycle jitter, VLYNQ5_CLK (output mode) (3)		250	ps
2	$t_{w(VLYNQ\_CLK\_H)}$	Pulse duration, VLYNQ5_CLK high (output mode) (3)	3.6		ns
3	$t_{w(VLYNQ\_CLK\_L)}$	Pulse duration, VLYNQ5_CLK low (output mode) (3)	3.6		ns
8	$t_{r(VTCKR)}$	Rise time, VLYNQ5_TX_D[1:0] and VLYNQ5_CLK (output mode) (3)		3	ns
9	$t_{f(VTCKF)}$	Fall time, VLYNQ5_TX_D[1:0] and VLYNQ5_CLK (output mode) (3)		3	ns
10	$t_{d(VCKH-VTH)}$	Delay time, VLYNQ5_CLK to VLYNQ5_TX_D[1:0] invalid	2.0		ns
11	$t_{d(VCKH-VTV)}$	Delay time, VLYNQ5_CLK to VLYNQ5_TX_D[1:0] valid		7.55	ns
End of Table 5-61					

1 The VLYNQ clock can be sourced internally or externally through the configuration bit CLK_DIR in the VLYNQ5 (CTRL) register. If sourced internally, this clock is based on the VBUSP_CLK.

2 See section 4 of Texas Instruments application report SPRA956, *Circuit-Board Design Guidelines for VLYNQ™ Devices,* to determine how to analyze VLYNQ timing.

3 Specified by design

Figure 5-52 VLYNQ Interface

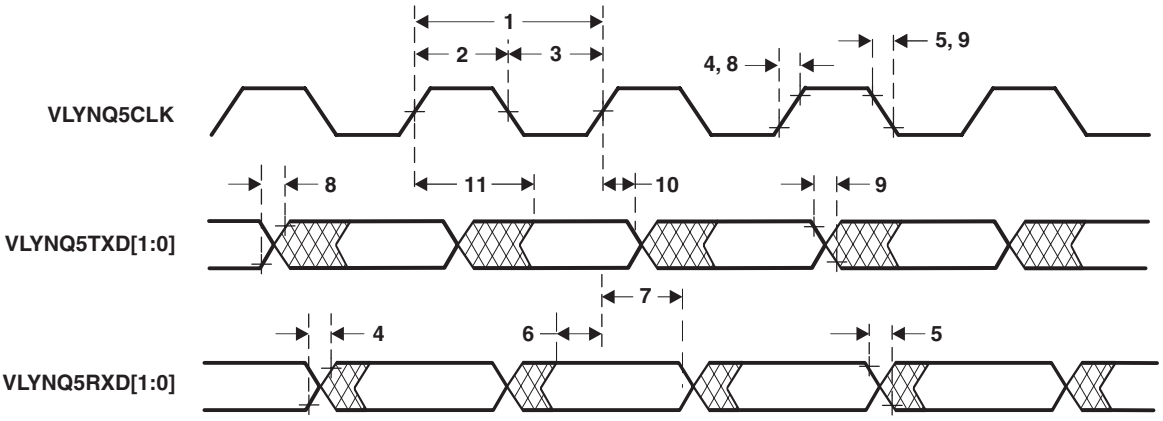


Figure 5-53 VLYNQ Interface (Five Terminal)

cmd1[7:4] pkttype	cmd1[3:0] adrmsk	cmd2[7:0]	bytecnt[7:4] (1 to 64)d	
0x0	0xF	not used	USED	Write
0x1	0xF	not used	USED	Write with Address Increment
0x2	X	not used	not used	Reserved
0x3	0xF	not used	not used	Write 32-bit Word with Address Increment
0x4	0xF	not used	USED	Configuration Write
0x5	0xF	not used	USED	Configuration Write with Address Increment
0x6	X	X	X	Reserved
0x7	0xF	not used	not used	Interrupt
0x8	0xF	not used	USED	Read
0x9	0xF	not used	USED	Read with Address Increment
0xA	X	not used	not used	Reserved
0xB	0xF	not used	not used	Read 32-bit Word with Address Increment
0xC	0xF	not used	USED	Configuration Read
0xD	0xF	not used	USED	Configuration Read with Address Increment
0xE	0xF	not used	USED	Read Response

	Code	8-bit	10-bit–	10-bit+
Flow Control Enable	/P/	0x1C	0x0F4	0x30B
Error Indication	/E/	0x3C	0x0F9	0x306
Flow Control Disable	/C/	0x5C	0x0F5	0x30A
Flowed	/F/	0x7C	0x0F3	0x30C
Initialization 0	/0/	0x9C	0x0F2	0x30D
Idle	/I/	0xBC	0x0FA	0x309
Initialization 1	/1/	0xDC	0x0F6	0x305
		0xFC	0x0F8	0x307
Byte Disable	/M/	0xF7	0x3A8	0x057
Start of Packet	/S/	0xFB	0x368	0x097
End of Packet	/T/	0xFD	0x2E8	0x117
Link	/L/	0xFE	0x1E8	0x217

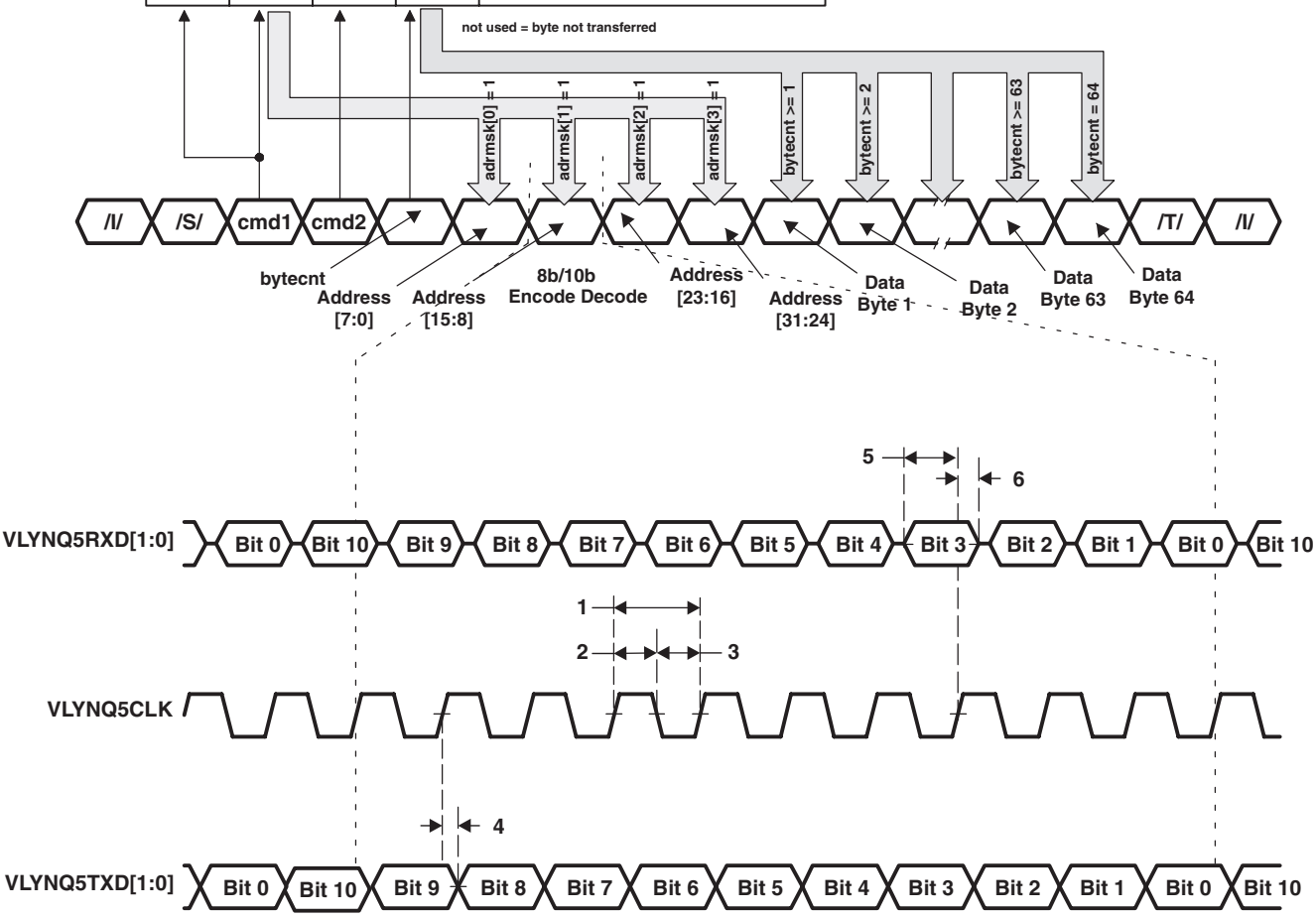


Figure 5-54 VLYNQ Equivalent Load Circuit

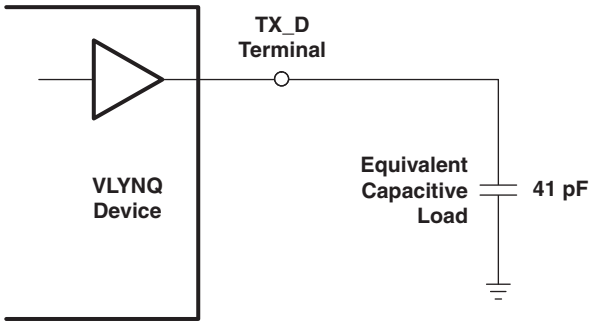


Figure 5-55 Derating Curve for $t_{d(VLYNQ\_CLK-VTH)}$

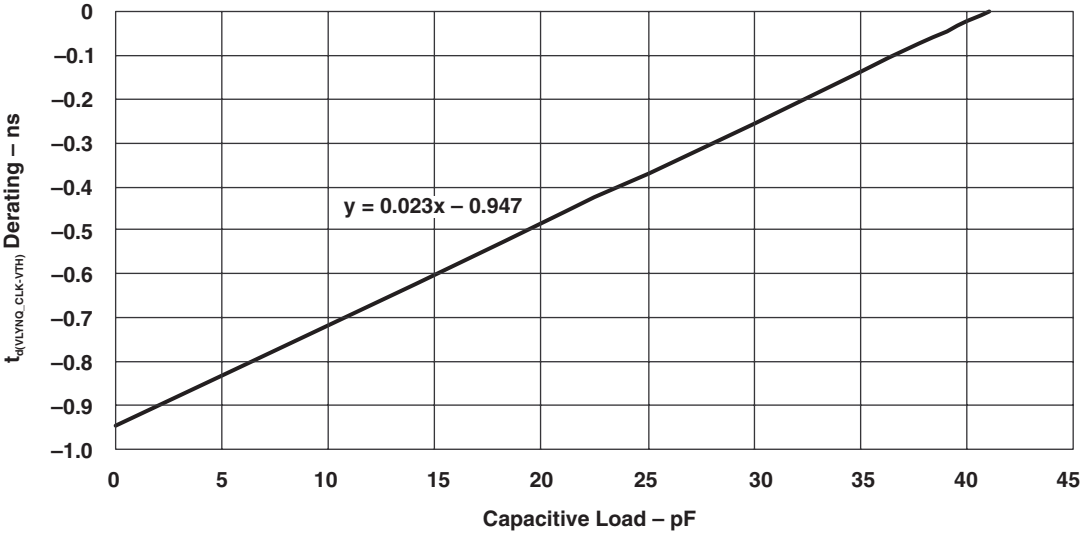
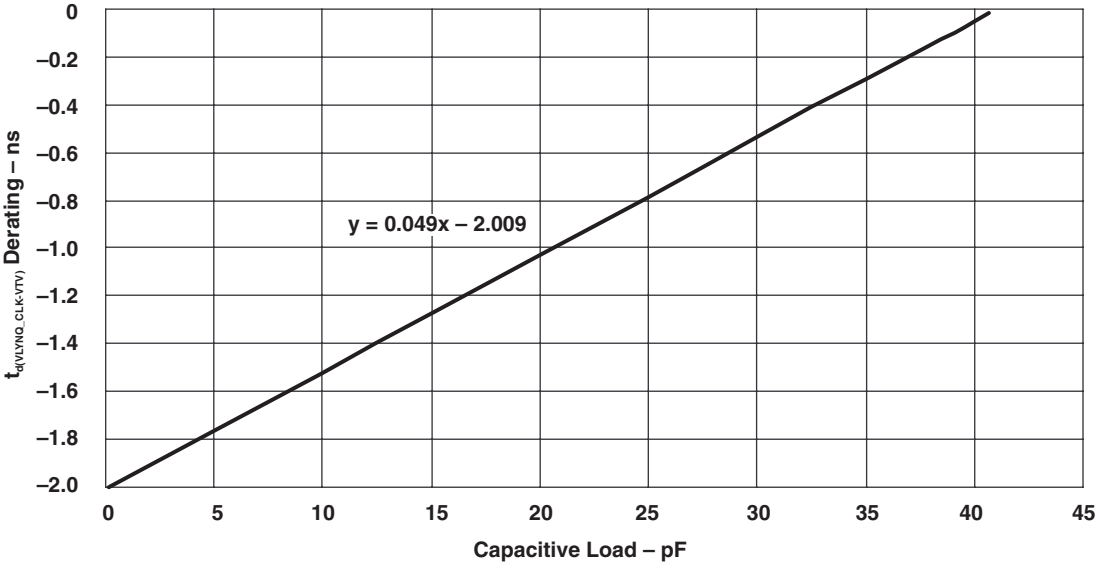


Figure 5-56 Derating Curve for $t_{d(VLYNQ\_CLK-VTV)}$



5.16 GPIO Timing

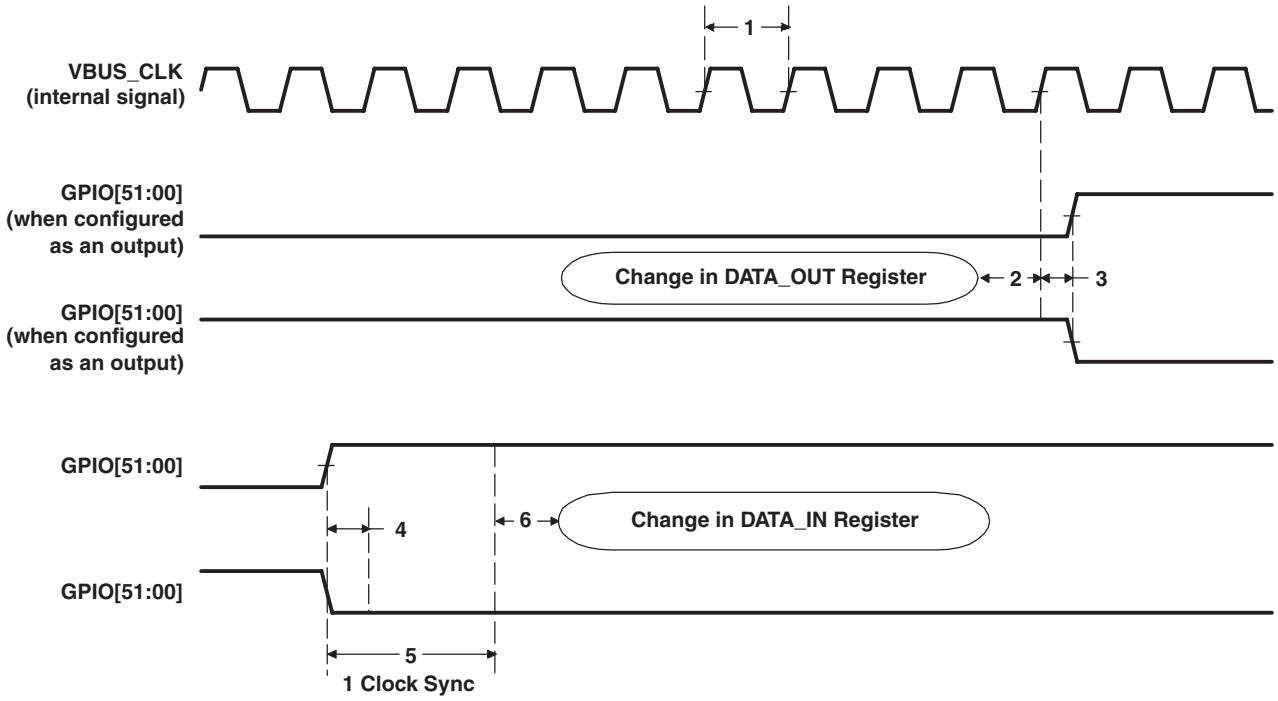
Table 5-62 GPIO Timing

See Figure 5-57					
No.	**Description**		**Min**	**Max**	**Unit**
	$f_{clock(VBUS\_CLK)}$	Clock frequency, VBUS_CLK [1]		62.5	MHz
1	$t_{c(VBUS\_CLK)}$	Cycle time, VBUS_CLK [1]	16		ns
2	$t_{d(GPIO\_O\_R)}$	Delay time, DATA_OUT register change to GPIO driver [1] [2]		0	ns
3	$t_{d(GPIO\_O)}$	Delay time, through GPIO driver to GPIO[51:00] output change [1] [2]	1	8	ns
4	$t_{d(GPIO\_I)}$	Delay time, GPIO[51:00]↑ (input) to VBUS_CLK↑ [1] [2]	$t_c \times 0$		ns
5	$t_{d(GPIO\_I)}$	Delay time, GPIO[51:00]↓ (input) to VBUS_CLK↓ [1] [2]	2		ns
6	$t_{d(GPIO\_I\_R)}$	Delay time, GPIO[51:00]↓ to DATA_IN register change (after one clock sync) [1] [2]		0	ns
End of Table 5-62					

1 Specified by design

2 The SYS_GPIO (DATA_IN) register contains raw data. This raw data is asynchronous, only having one VBUS_CLK delay, instead of two. In addition, this data is not latched in the register and is free to change when there is a change to the GPIO signal.

Figure 5-57 GPIO



5.17 Keypad Interface Timing

Table 5-63 Keypad Timing

See Figure 5-58					
No.	**Description (1) (2)**		**Min**	**Max**	**Unit**
	$f_{clock(VBUS\_CLK)}$	Clock frequency, VBUS_CLK		62.5	MHz
1	$t_{c(VBUS\_CLK)}$	Cycle time, VBUS_CLK	16		ns
2	$t_{d(KEYPAD\_O\_R)}$	Delay time, DATA_OUT register to VBUS_CLK↑ (3) (4)		0	Clock
3	$t_{d(KEYPAD\_O)}$	Delay time, VBUS_CLK↑ to KEYPAD(15:00)↑ (4)	1	8	ns
4	$t_{d(KEYPAD\_I)}$	Delay time, KEYPAD[15:00]↑ input to VBUS_CLK↑ (4)	0		ns
5	$t_{d(KEYPAD\_I)}$	Delay time, KEYPAD[15:00]↓ input to VBUS_CLK↓ (4)	$t_c \times 2$		ns
6	$t_{d(KEYPAD\_I\_R)}$	Delay time, VBUSA_CLK↓ to DATA_IN register change after one clock sync (4)		0	ns
End of Table 5-63					

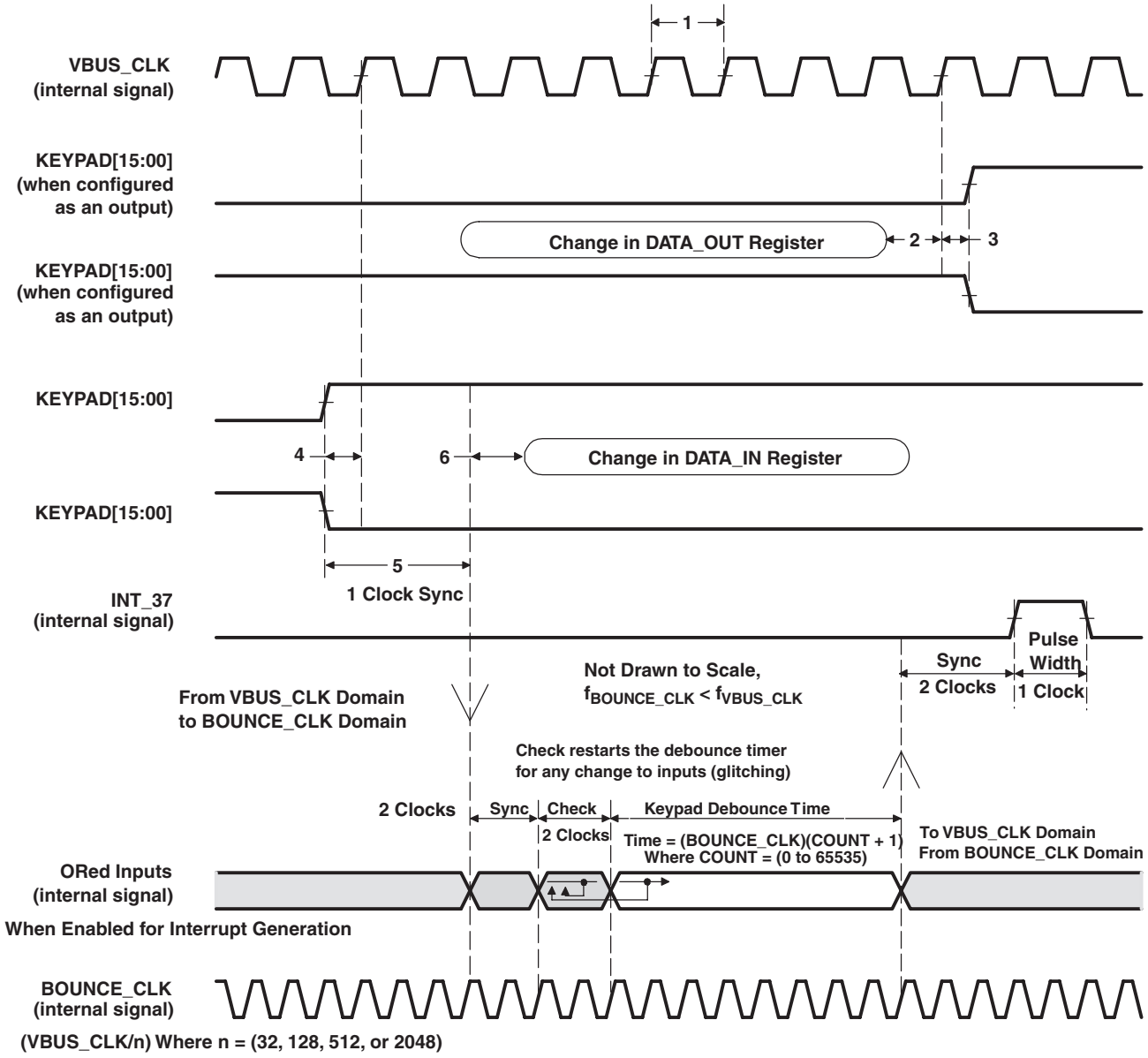
1 The debounce counter can be used to filter keypad activation and deactivation mechanical glitches. The filtered results feed the keypad interrupt to the MIPS. Prior to use, the keypad I/O must be properly enabled and polarized through the KEYPAD (MSK_POLARITY) register. The debounce time is defined in the KEYPAD (CNT) register. Additional control is required in the KEYPAD (CTRL) register.

2 The KEYPAD (DATA_IN) register contains raw data. This raw data is asynchronous, only having one VBUS_CLK delay, instead of two. In addition, this data is not latched in the register and is free to change when there is a change to the KEYPAD signal.

3 This value is one VBUS_CLK cycle time.

4 Specified by design

Figure 5-58 Keypad



5.18 MIPS and DSP Interrupt Interface Timing

There are five external MIPS interrupt sources.

EXT_INT[4:1] enter the MIPS interrupt controller as INT_4 to INT_1, while TELE_INT enters as INT_23.

The MIPS interrupt interface is asynchronous. Input data is synchronized with two VBUSP_CLK cycles upon entry to the TNETV1056.

The SYS_INT (STAT_RAW_1) and SYS_INT (STAT_RAW_2) register set holds the interrupt pending status of all TNETV1056 interrupts destined for the MIPS. To generate a MIPS interrupt, the corresponding bit in the SYS_INT (STAT_MSK_1) or SYS_INT (STAT_MSK_2) register set must also be active.

The polarity (active high or low) may be configured in the SYS_INT (POLARITY_1 and SYS_INT (POLARITY_2) register set. The type (active level or edge) may be configured in the SYS_INT (TYPE_1) and SYS_INT (TYPE_2) register set.

TELE_INT is the only external DSP interrupt source.

The DSP interrupt interface is asynchronous. Input data is synchronized with two DSP_CLK cycles upon entry to the TNETV1056 DSP subsystem.

The DSP_INT (IFR0) and DSP_INT (IFR1) register set holds the interrupt pending status of all TNETV1056 interrupts destined for the DSP. To generate a DSP interrupt, the corresponding bit in the DSP_INT (IER0) or DSP_INT (IER1) register set also must be active.

The input polarity is a fixed active high, and the input type is a fixed active edge.

Table 5-64 MIPS Interrupt Timing

See Figure 5-59					
No.		**Description**	**Min**	**Max**	**Unit**
	$f_{clock(VBUSP\_CLK)}$	Clock frequency, VBUSP_CLK		125	MHz
1	$t_{c(VBUSP\_CLK)}$	Cycle time, VBUSP_CLK	8		ns
2	$t_{d(INT)}$	Delay time, EXT_INT[4:1]/TELE_INT↑ to VBUSP_CLK↑ (1)	0		ns
3	$t_{d(INT\_E)}$	Delay time, VBUSP_CLK↑ to EXT_INT[4:1]/TELE_INT edge (↑/↓) (1)	$t_c \times 3$		ns
4	$t_{d(INT\_L)}$	Delay time, VBUSP_CLK↑ to EXT_INT[4:1]/TELE_INT level (H/L) (1)	$t_c \times 3$		ns
5	$t_{d(INT\_R)}$	Delay time, MIPS interrupt (after synchronization) to active status in the STAT_RAW register	$t_c \times 1$		ns
End of Table 5-64					

1 Specified by design

Figure 5-59 MIPS Interrupt

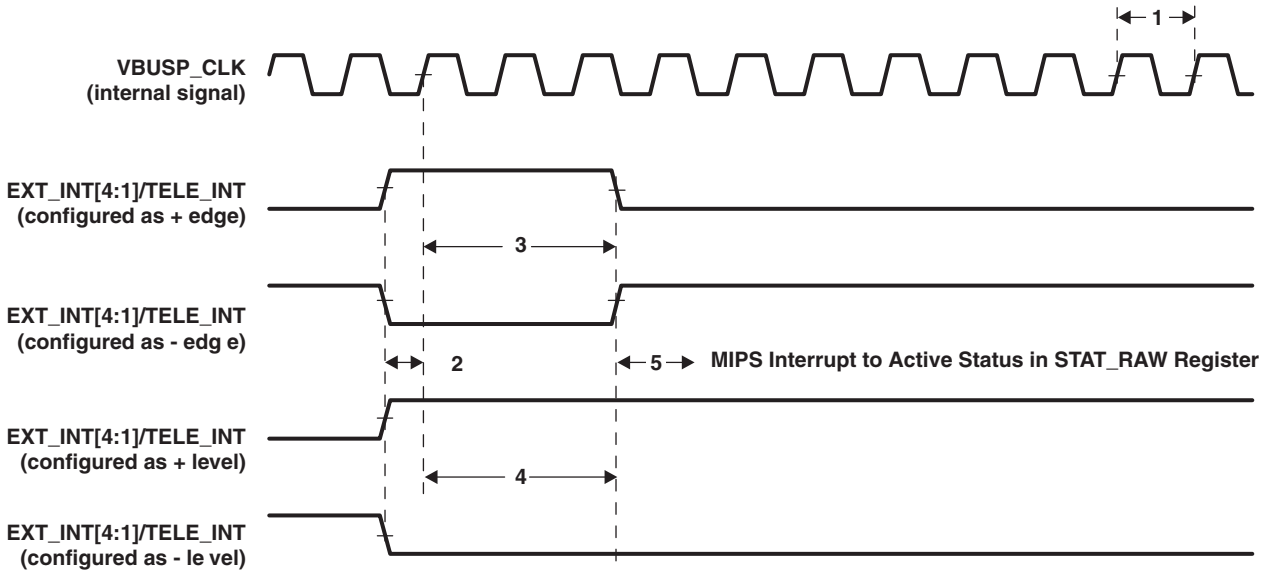
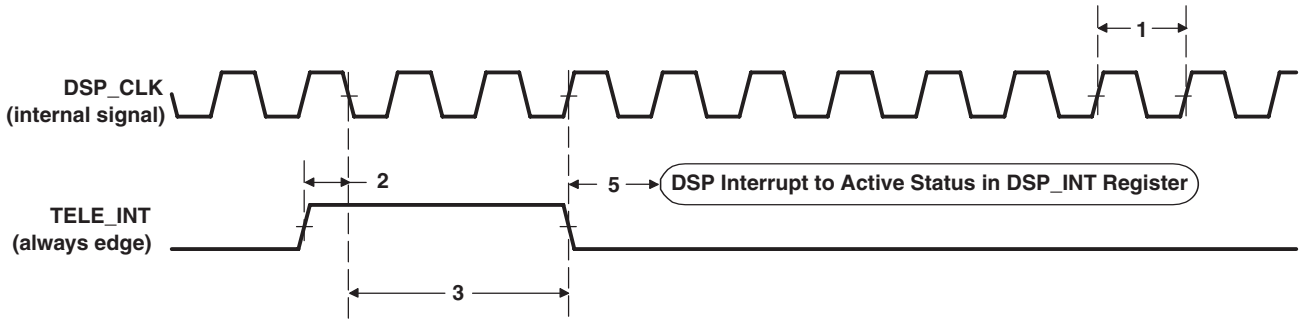


Table 5-65 DSP Interrupt Timing

See Figure 5-60					
No.	**Description**		**Min**	**Max**	**Unit**
	$f_{clock(DSP\_CLK)}$	Clock frequency, DSP_CLK		100	MHz
1	$t_{c(DSP\_CLK)}$	Cycle time, DSP_CLK	10		ns
2	$t_{d(DSP\_INT)}$	Delay time, TELE_INT↑ to DSP_CLK↓ (1)	0		ns
3	$t_{d(DSP\_INT\_E)}$	Delay time, DSP_CLK↓ to TELE_INT↓ (1)	$t_c \times 3$		ns
5	$t_{d(DSP\_INT\_R)}$	Delay time, DSP interrupt (after synchronization) to active status in DSP_INT register (1)	$t_c \times 1$		ns
End of Table 5-65					

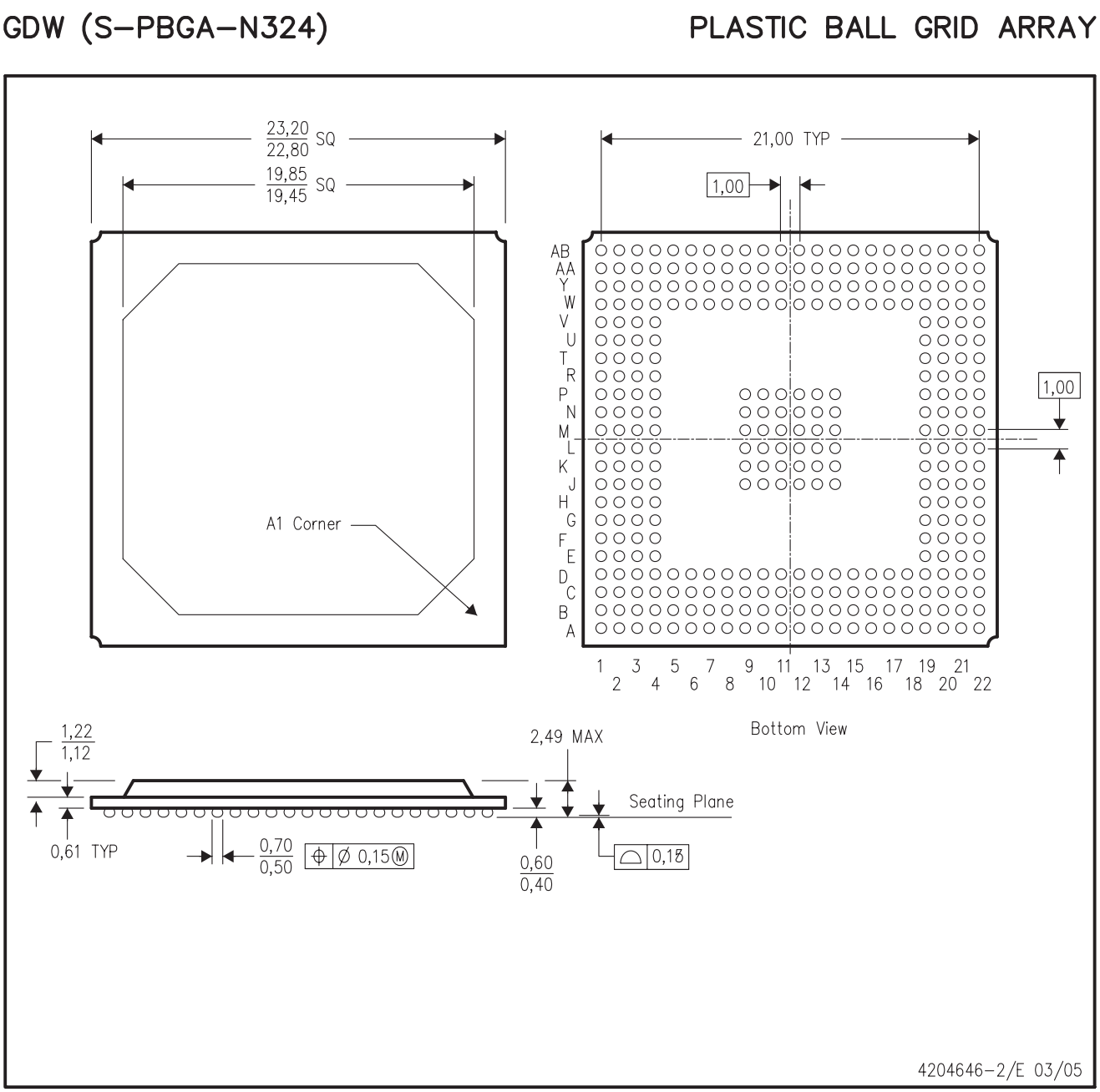
1 Specified by design

Figure 5-60 DSP Interrupt



6 Mechanical Specification

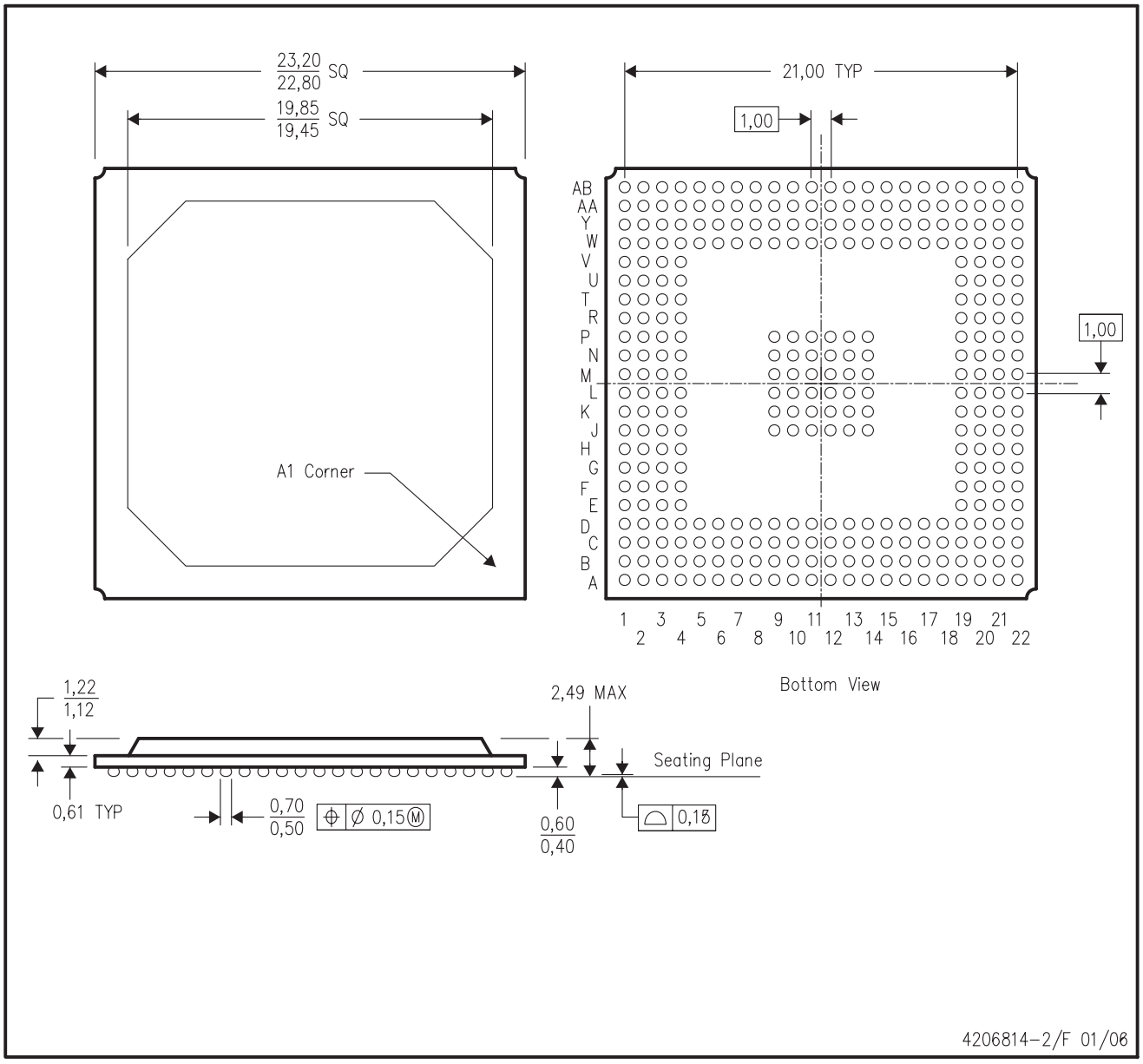
Figure 6-1 GDW (S-PBGA-N324) Plastic Ball Grid Array



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–151
D. Thermally enhanced plastic package

Figure 6-2 ZDW (S-PBGA-N324) Pb-Free Plastic Ball Grid Array

ZDW (S–PBGA–N324) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–151
D. Thermally enhanced plastic package
E. This package is a lead free solder ball design.

7 Documentation Support

Table 7-1 Documentation (Part 1 of 2)

Name Description	Literature Number	Location	TNETV1056 Function
TNETV1056 **Data Manual** TNETV1056 features, I/O, hardware overview, and electrical specification	SPRS258C	www.ti.com	All
TNETV1050 User's Guide TNETV1050/1055/1056/1060/1062/1015 feature detail including register description	SPRU799	www.ti.com	All
TMS320C55x™ DSP Functional Overview Basic overview of TMS320 C55x™ DSP core	SPRU312	www.ti.com	DSP
TMS320C55x™ DSP CPU Reference Guide Detailed description of C55x CPU architecture, registers, memory, stack, interrupts and addressing	SPRU371	www.ti.com	DSP
TMS320C55x™ DSP Peripherals Reference Guide Detailed description of C55x peripherals, including the McBSP	SPRU317	www.ti.com	DSP
TMS320C55x™ DSP Programmer's Guide Explanation and examples of Assembly and C code optimization (including DSPLIB), fixed-point arithmetic, and bit-reversed addressing for the C55x	SPRU376	www.ti.com	DSP
TMS320C55x™ DSP Mnemonic Instruction Set Reference Guide Summary, description, and opcodes for the mnemonic form of the C55x instruction set	SPRU374	www.ti.com	DSP
TMS320C55x™ DSP Algebraic Instruction Set Reference Guide Summary, description, and opcodes for the algebraic form of the C55x instruction set	SPRU375	www.ti.com	DSP
TMS320C55x™ Optimizing C Compiler User's Guide Detailed explanation of how to use the compiler, optimizer, interlist utility, library-build utility, and C++ name demangler for the C55x DSP	SPRU281	www.ti.com	DSP
TMS320C55x™ Assembly Language Tools User's Guide	SPRU280	www.ti.com	DSP
TMS320C55x™ DSP Library Programmer's Reference Detailed explanation of the C55x DSP library (DSPLIB) and its use	SPRU422	www.ti.com	DSP
Code Composer Studio™ User's Guide Explanation of how to use Code Composer Studio to develop and debug real-time software applications	SPRU393	www.ti.com	DSP
TMS320C55x™ DSP Technical Overview Detailed overview of the C55x DSP core	SPRU328	www.ti.com	DSP
MIPS32™ 4KE™ Processor Core Family Software User's Manual Description of the MIPS32 4KE processor and functions necessary for coding	MD00103	www.mips.com	MIPS Processor
MIPS32™ 4KE™ Processor Core Family Integrator's Guide Targeted for the ASIC designer who is integrating the MIPS32 4KE processor core into the system ASIC	MD00104	www.mips.com	MIPS Processor
MIPS32™ 4KEc™ Processor Core Data Sheet MIPS32 4KEc features, I/O, hardware overview, and electrical specification	MD00111	www.mips.com	MIPS Processor
ECt Interface Specification Describes the ECt interface designed for microprocessor cores	MD00052	www.mips.com	MIPS Processor

Table 7-1 Documentation (Part 2 of 2)

Name Description	Literature Number	Location	TNETV1056 Function
Core Coprocessor Interface Specification Describes the coprocessor interface standard supported by MIPS32 processor core	MD00068	www.mips.com	MIPS Processor
EJTAG Specification Describes the behavior and organization of on-chip EJTAG hardware resources as seen by software and by external agents	MD00047	www.mips.com	MIPS JTAG
EJTAG Implementation Application Note Practical guide to assist in achieving the maximum possible performance in terms of speed and reliability over the JTAG serial link	MD00071	www.mips.com	MIPS JTAG
EJTAG Trace Control Block Specification Detailed explanation of tracing logic within the MIPS32 4KEc JTAG	MD00148	www.mips.com	MIPS JTAG
MIPS32™Architecture for Programmers, Volume III: The MIPS32™ Privileged Resource Architecture Describes the MIPS32 Privileged Resource Architecture, which defines and governs the behavior of the privileged resources included in a MIPS32 processor implementation	MD00090	www.mips.com	MIPS
TLV320AIC20 Data Manual Register-level description of the TLV320AIC20 CODEC (not exact implementation for TNETV1056)	SLAS363A	www.ti.com	AIC20 Codec
MystiPHY™ 110 10/100 Base-TX/FX Ethernet PHY Core Product Brief Short description of PHY features and structure	MystiPHY110	www.mysticom.com	PHY